

FEATURES:

- Organized as 128K x8 / 256K x8 / 512K x8
- Single 4.5-5.5V Read and Write Operations
- Superior Reliability
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- Low Power Consumption (typical values at 14 MHz)
 - Active Current: 10 mA (typical)
 - Standby Current: 30 µÅ (typical)
- Sector-Erase Capability
 - Uniform 4 KByte sectors
- Fast Read Access Time:
 - 55 ns
 - 70 ns
- Latched Address and Data
- Automatic Write Timing
 - Internal VPP Generation

• Fast Erase and Byte-Program

- Sector-Erase Time: 18 ms (typical)
- Chip-Erase Time: 70 ms (typical)
- Byte-Program Time: 14 µs (typical)
- Chip Rewrite Time:
 2 seconds (typical) for SST39SF010A
 4 seconds (typical) for SST39SF020A
 8 seconds (typical) for SST39SF040
- End-of-Write Detection
 - Toggle Bit
 - Data# Polling
- TTL I/O Compatibility
- JEDEC Standard
 - Flash EEPROM Pinouts and command sets
- Packages Available
- 32-lead PLCC
- 32-lead TSOP (8mm x 14mm)
- 32-pin PDIP
- All devices are RoHS compliant
- All non-Pb (lead-free) devices are RoHS compliant

PRODUCT DESCRIPTION

The SST39SF010A/020A/040 are CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A/040 devices write (Program or Erase) with a 4.5-5.5V power supply. The SST39SF010A/020A/040 devices conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39SF010A/020A/040 devices provide a maximum Byte-Program time of 20 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF010A/020A/040 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39SF010A/020A/040 are offered in 32-lead PLCC and 32-lead TSOP packages. A 600 mil, 32-pin PDIP is also available. See Figures 2, 3, and 4 for pin assignments.



Data Sheet

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39SF010A/020A/040 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram (Figure 5) for further details.

Byte-Program Operation

The SST39SF010A/020A/040 are programmed on a byteby-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 6 and 7 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H)

is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 10 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Chip-Erase Operation

The SST39SF010A/020A/040 provide Chip-Erase operation, which allows the user to erase the entire memory array to the "1s" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a sixbyte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 19 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST39SF010A/020A/040 provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.



Data# Polling (DQ7)

When the SST39SF010A/020A/040 are in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ7 will produce a '0'. Once the internal Erase operation is completed, DQ7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 17 for a flowchart.

Toggle Bit (DQ₆)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 17 for a flowchart.

Data Protection

The SST39SF010A/020A/040 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

<u>Noise/Glitch Protection:</u> A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

 $\underline{V_{DD}}$ Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.5V.

<u>Write Inhibit Mode:</u> Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39SF010A/020A/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST39SF010A/ 020A/040 devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC} .

Product Identification

The Product Identification mode identifies the device as the SST39SF040, SST39SF010A, or SST39SF020A and manufacturer as SST. This mode may be accessed by software operations. Users may wish to use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, Table 4 for software operation, Figure 12 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart.

TABLE 1: Product Identification

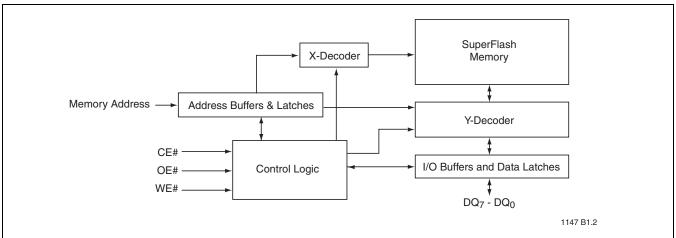
	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39SF010A	0001H	B5H
SST39SF020A	0001H	B6H
SST39SF040	0001H	B7H

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Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform and Figure 18 for a flowchart.







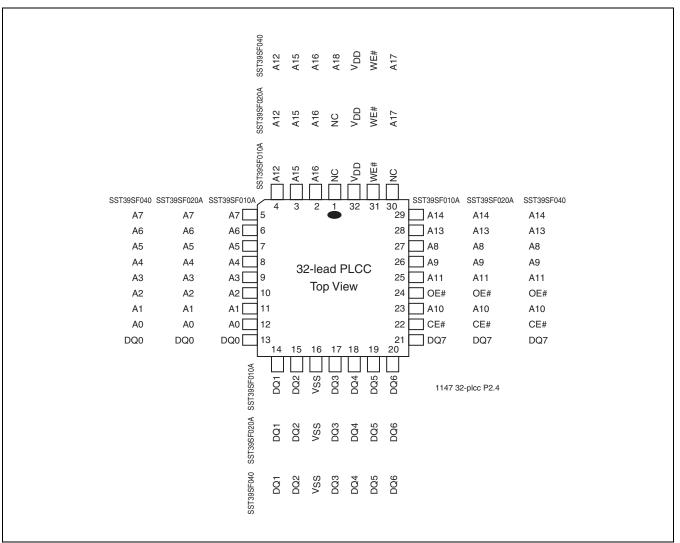
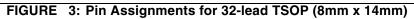
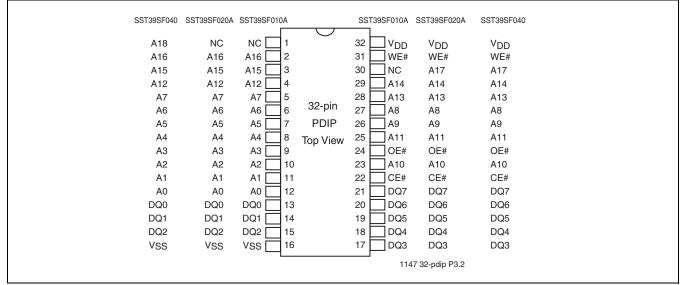


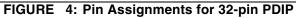
FIGURE 2: Pin Assignments for 32-lead PLCC



Ś	SST39SF040	SST39SF020A	SST39SF010A		S	ST39SF010A	SST39SF020A	SST39SF040
	A11	A11	A11 1	2	32	OE#	OE#	OE#
	A9	A9	A9 2)	31	A10	A10	A10
	A8	A8	A8 🔤 3		30	CE#	CE#	CE#
	A13	A13	A13 4		29	DQ7	DQ7	DQ7
	A14	A14	A14 📩 5		28	DQ6	DQ6	DQ6
	A17	A17	NC 6	Standard Pinout	27	DQ5	DQ5	DQ5
	WE#	WE#	WE# 7	—	26	DQ4	DQ4	DQ4
	V _{DD}	V _{DD}	V _{DD} 8	Top View	25	DQ3	DQ3	DQ3
	A18	NC	NC 9	D: 11	24	Vss	VSS	V _{SS}
	A16	A16	A16 10	Die Up	23	DQ2	DQ2	DQ2
	A15	A15	A15 11		22	DQ1	DQ1	DQ1
	A12	A12	A12 12		21	DQ0	DQ0	DQ0
	A7	A7	A7 13		20	A0	A0	A0
	A6	A6	A6 14		19	A1	A1	A1
	A5	A5	A5 15		18	A2	A2	A2
	A4	A4	A4 💶 16		17	A3	A3	A3
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Data Sheet

TABLE 2: Pin Description

Symbol	Pin Name	Functions	
A _{MS} ¹ -A ₀	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS} - A_{12} address lines will select the sector.	
DQ ₇ -DQ ₀	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.	
CE#	Chip Enable	To activate the device when CE# is low.	
OE#	Output Enable	To gate the data output buffers.	
WE#	Write Enable	To control the Write operations.	
V _{DD}	Power Supply	To provide 5.0V supply (4.5-5.5V)	
V _{SS}	Ground		
NC	No Connection	Unconnected pins.	
			T2.2 114

1. A_{MS} = Most significant address

 $A_{MS} = A_{16}$ for SST39SF010A, A_{17} for SST39SF020A, and A_{18} for SST39SF040

Mode	CE#	OE#	WE#	DQ	Address
Read	VIL	V _{IL}	V _{IH}	D _{OUT}	A _{IN}
Program	VIL	VIH	VIL	D _{IN}	A _{IN}
Erase	V _{IL}	V _{IH}	V _{IL}	X ¹	Sector address, XXH for Chip-Erase
Standby	VIH	Х	Х	High Z	х
Write Inhibit	х	VIL	Х	High Z/ D _{OUT}	х
	х	Х	VIH	High Z/ D _{OUT}	х
Product Identification					
Software Mode	VIL	VIL	VIH		See Table 4

TABLE 3: Operation Modes Selection

1. X can be V_{IL} or V_{IH} , but no other value.

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Command Sequence	1st E Write (2nd E Write C		3rd E Write (4th E Write (5th B Write C		6th E Write C	
	Addr ¹	Data	Addr ¹	Data								
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA ²	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA _X ³	30H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry ^{4,5}	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit ⁶	XXH	F0H										
Software ID Exit ⁶	5555H	AAH	2AAAH	55H	5555H	F0H						
												T4.2 1147

TABLE 4: Software Command Sequence

 Address format A₁₄-A₀ (Hex), Addresses A_{MS}-A₁₅ can be V_{IL} or V_{IH}, but no other value, for the Command sequence. A_{MS} = Most significant address

 $A_{MS} = A_{16}$ for SST39SF010A, A_{17} for SST39SF020A, and A_{18} for SST39SF040

2. BA = Program Byte address

3. SA_X for Sector-Erase; uses A_{MS} - A_{12} address lines

4. The device does not remain in Software Product ID mode if powered down.

5. With A_{MS} - A_1 = 0; SST Manufacturer's ID = BFH, is read with A_0 = 0,

SST39SF010A Device ID = B5H, is read with $A_0 = 1$ SST39SF020A Device ID = B6H, is read with $A_0 = 1$

SST39SF040 Device ID = B7H, is read with $A_0 = 1$

6. Both Software ID Exit operations are equivalent

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	
Storage Temperature	
D. C. Voltage on Any Pin to Ground Potential	
Transient Voltage (<20 ns) on Any Pin to Ground Potential	
Voltage on A ₉ Pin to Ground Potential	
Package Power Dissipation Capability (Ta = 25°C)	
Through Hold Lead Soldering Temperature (10 Seconds)	
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ¹	
1. Outputs shorted for no more than one second. No more than one output shorted at a time.	

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Operating Range

Range	Ambient Temp	V _{DD}
Commercial	0°C to +70°C	4.5-5.5V
Industrial	-40°C to +85°C	4.5-5.5V

AC Conditions of Test

Input Rise/Fall Time 5 ns	
Output Load $C_L =$	30 pF for 55 ns
Output Load $C_L =$	100 pF for 70 ns
See Figures 14 and 15	





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TABLE 5: DC Operating Characteristics V_{DD} = 4.5-5.5V¹

		Limits			
Symbol	Parameter	Min	Мах	Units	Test Conditions
I _{DD}	Power Supply Current				Address input=V _{ILT} /V _{IHT} , at f=1/T _{RC} Min V_{DD} =V _{DD} Max
	Read ²		25	mA	CE#=VIL, OE#=WE#=VIH, all I/Os open
	Program and Erase		35	mA	CE#=WE#=V _{IL} , OE#=V _{IH}
I _{SB1}	Standby V _{DD} Current (TTL input)		3	mA	CE#=V _{IH} , V _{DD} =V _{DD} Max
I _{SB2}	Standby V _{DD} Current (CMOS input)		100	μA	CE#=V _{IHC} , V _{DD} =V _{DD} Max
ILI	Input Leakage Current		1	μA	V _{IN} =GND to V _{DD} , V _{DD} =V _{DD} Max
I _{LO}	Output Leakage Current		10	μA	V _{OUT} =GND to V _{DD} , V _{DD} =V _{DD} Max
V _{IL}	Input Low Voltage		0.8	V	V _{DD} =V _{DD} Min
VIH	Input High Voltage	2.0		V	V _{DD} =V _{DD} Max
VIHC	Input High Voltage (CMOS)	V _{DD} -0.3		V	V _{DD} =V _{DD} Max
V _{OL}	Output Low Voltage		0.4	V	I _{OL} =2.1 mA, V _{DD} =V _{DD} Min
V _{OH}	Output High Voltage	2.4		V	I _{OH} =-400 μA, V _{DD} =V _{DD} Min

 Typical conditions for the Active Current shown on the front data sheet page are average values at 25°C (room temperature), and V_{DD} = 5V for SF devices. Not 100% tested.

2. Values are for 70 ns conditions. See the Multi-Purpose Flash Power Rating application note for further information.

TABLE 6: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
T _{PU-READ} ¹	Power-up to Read Operation	100	μs
T _{PU-WRITE} ¹	Power-up to Program/Erase Operation	100	μs
			T6.1 1147

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: Capacitance (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C _{I/O} ¹	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
C _{IN} ¹	Input Capacitance	$V_{IN} = 0V$	6 pF
			T7.0 1147

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N _{END} ^{1,2}	Endurance	10,000	Cycles	JEDEC Standard A117
T _{DR} ¹	Data Retention	100	Years	JEDEC Standard A103
ILTH ¹	Latch Up	100 + I _{DD}	mA	JEDEC Standard 78

T8.2 1147 1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2. N_{END} endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.

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AC CHARACTERISTICS

TABLE9: Read Cycle Timing Parameters $V_{DD} = 4.5-5.5V$

		SST39SF010A/020A/040-55		SST39SF010A/020A/040-70		
Symbol	Parameter	Min	Max	Min	Max	Units
T _{RC}	Read Cycle Time	55		70		ns
T _{CE}	Chip Enable Access Time		55		70	ns
T _{AA}	Address Access Time		55		70	ns
T _{OE}	Output Enable Access Time		30		35	ns
T _{CLZ} 1	CE# Low to Active Output	0		0		ns
T _{OLZ} 1	OE# Low to Active Output	0		0		ns
T _{CHZ} 1	CE# High to High-Z Output		15		25	ns
T _{OHZ} 1	OE# High to High-Z Output		15		25	ns
T _{OH} 1	Output Hold from Address Change	0		0		ns
	•	•	-			T9.4 1147

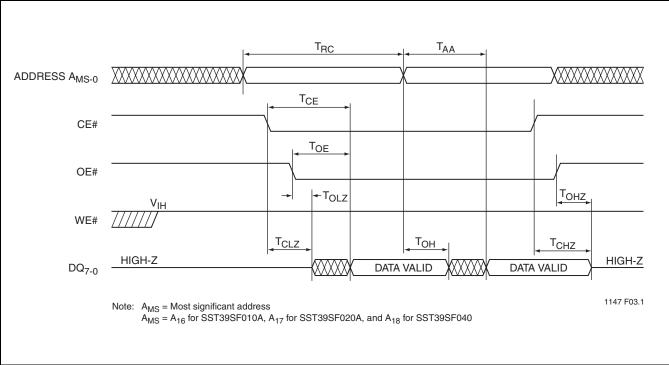
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

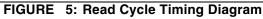
Symbol Parameter Min Max Units T_{BP} Byte-Program Time 20 μs T_{AS} Address Setup Time 0 ns Address Hold Time T_{AH} 30 ns T_{CS} WE# and CE# Setup Time 0 ns WE# and CE# Hold Time Тсн 0 ns TOES **OE# High Setup Time** 0 ns TOEH **OE# High Hold Time** 10 ns T_{CP} **CE# Pulse Width** 40 ns Twp WE# Pulse Width 40 ns T_{WPH}¹ WE# Pulse Width High 30 ns T_{CPH}¹ CE# Pulse Width High 30 ns Data Setup Time T_{DS} 40 ns T_{DH}^{1} Data Hold Time 0 ns T_{IDA}¹ Software ID Access and Exit Time 150 ns Sector-Erase T_{SE} 25 ms $\mathsf{T}_{\mathsf{SCE}}$ Chip-Erase 100 ms T10.1 1147

TABLE 10: Program/Erase Cycle Timing Parameters

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.







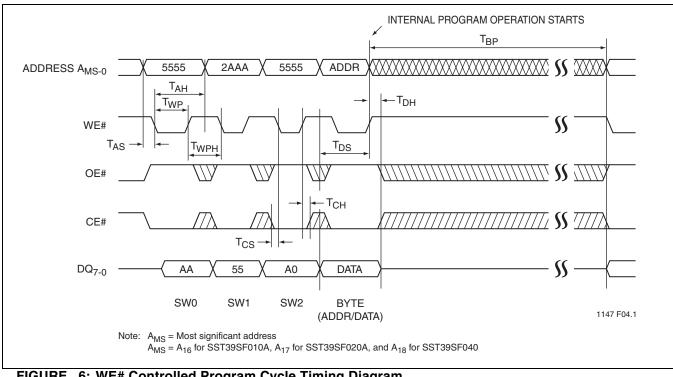


FIGURE 6: WE# Controlled Program Cycle Timing Diagram



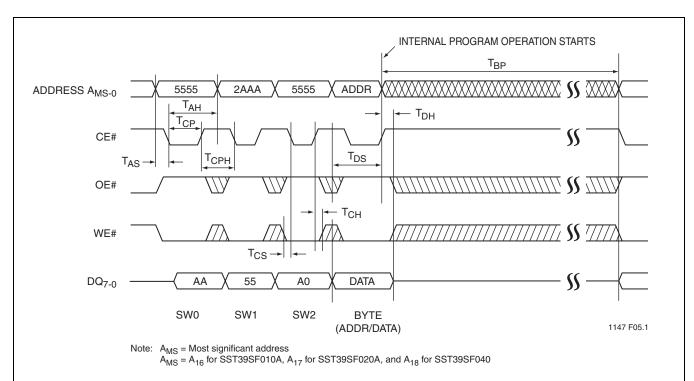


FIGURE 7: CE# Controlled Program Cycle Timing Diagram

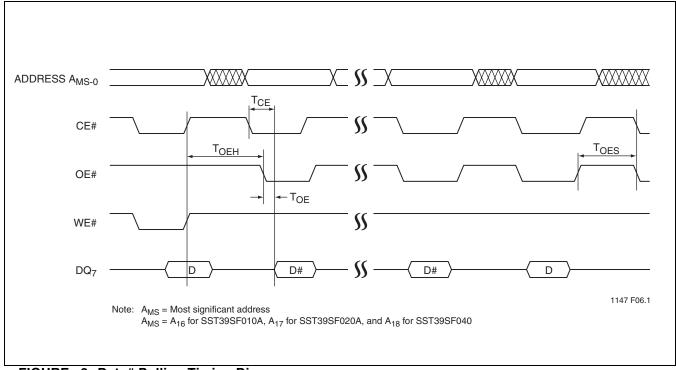
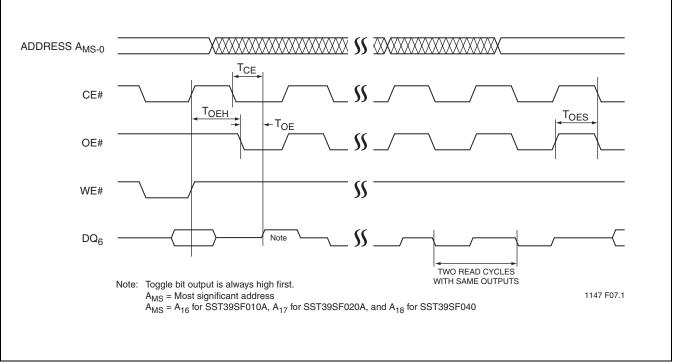


FIGURE 8: Data# Polling Timing Diagram







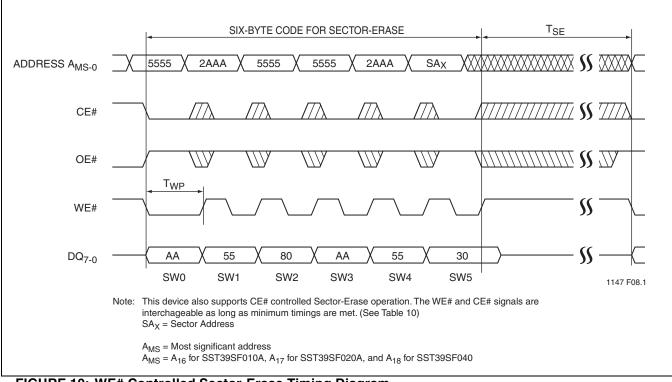
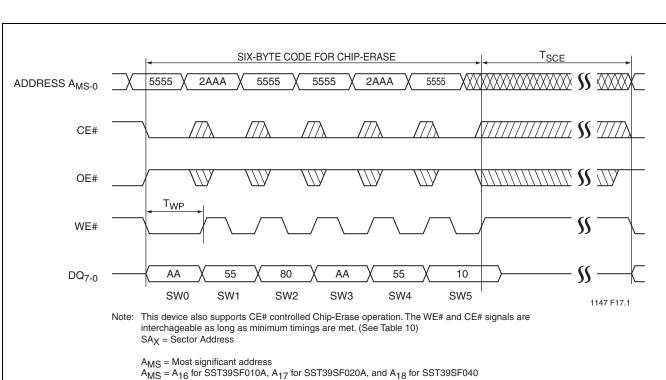


FIGURE 10: WE# Controlled Sector-Erase Timing Diagram





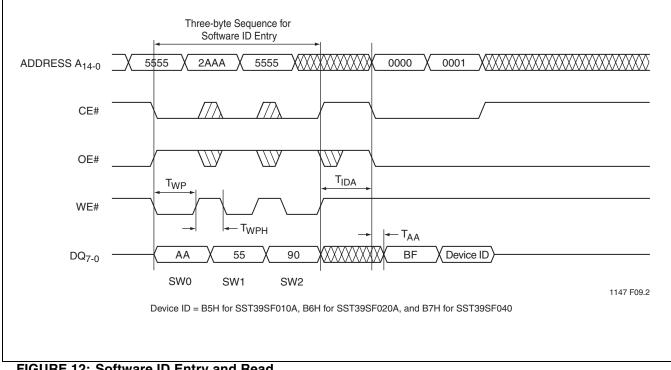


FIGURE 12: Software ID Entry and Read





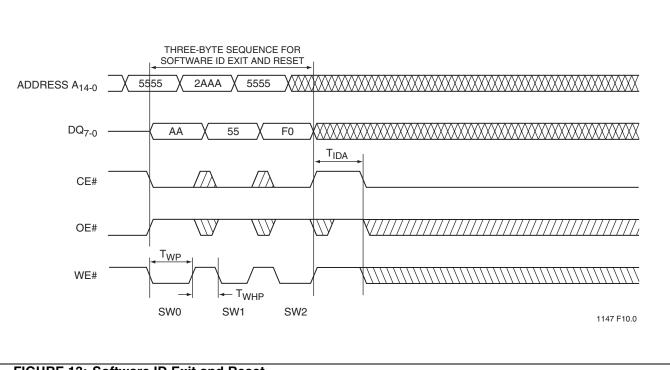
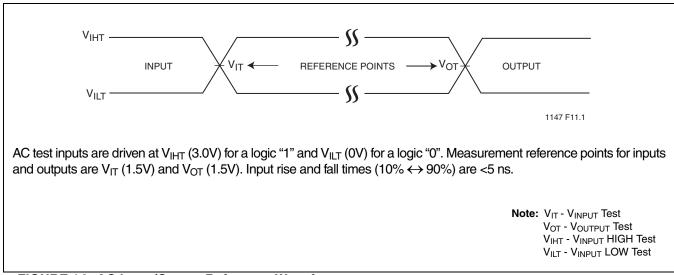
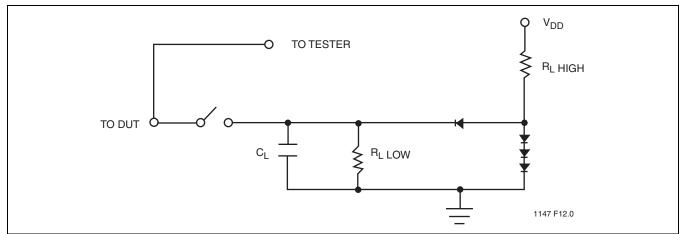


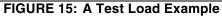
FIGURE 13: Software ID Exit and Reset













1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

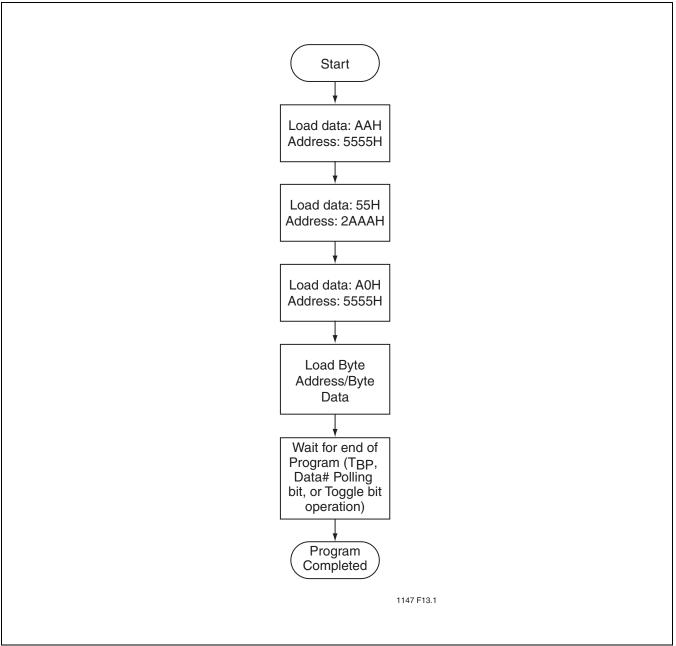
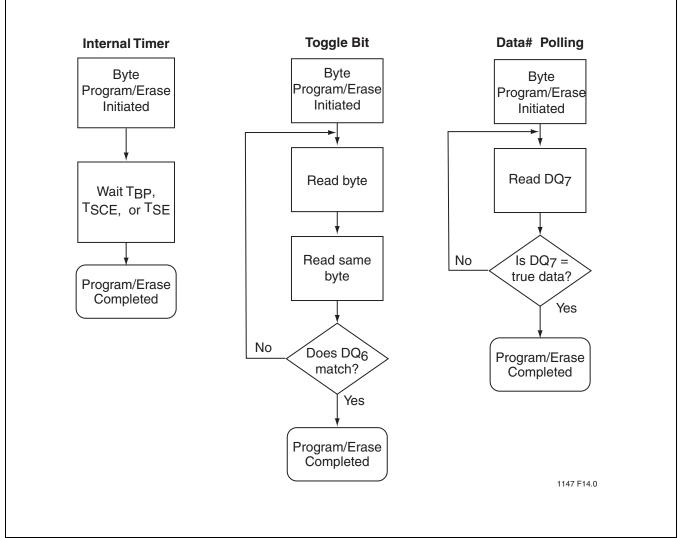
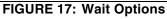


FIGURE 16: Byte-Program Algorithm









1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash SST39SF010A / SST39SF020A / SST39SF040

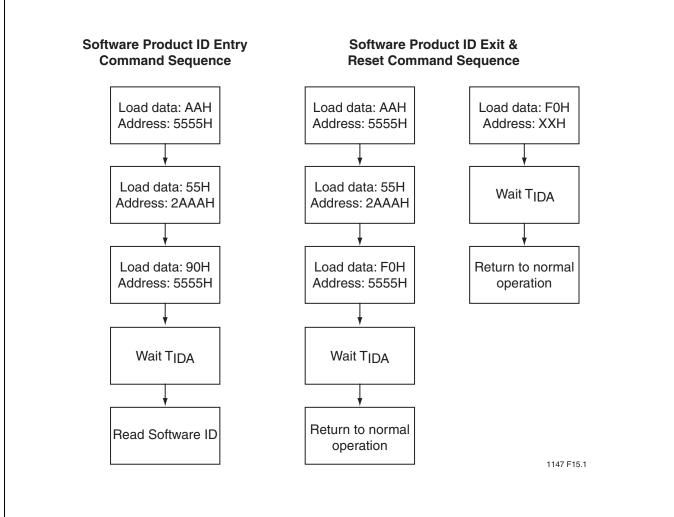


FIGURE 18: Software Product Command Flowcharts



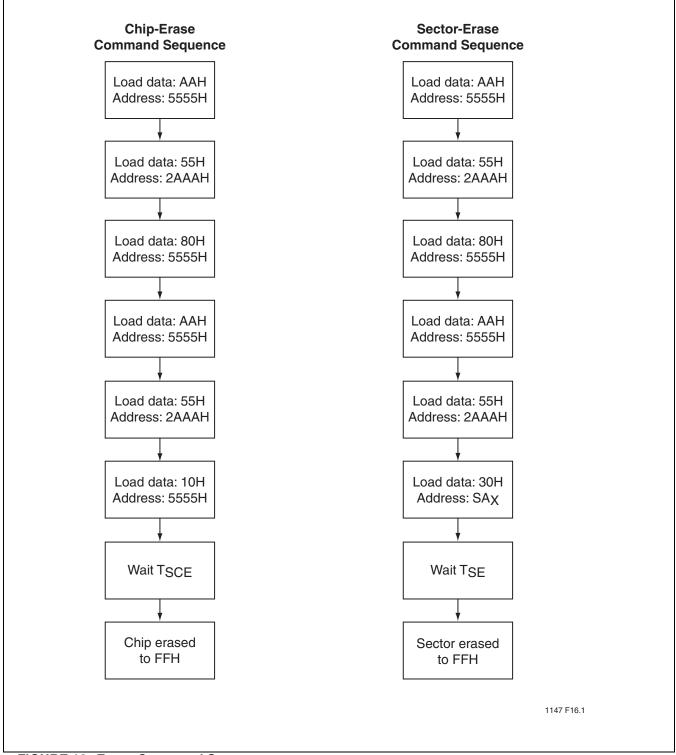
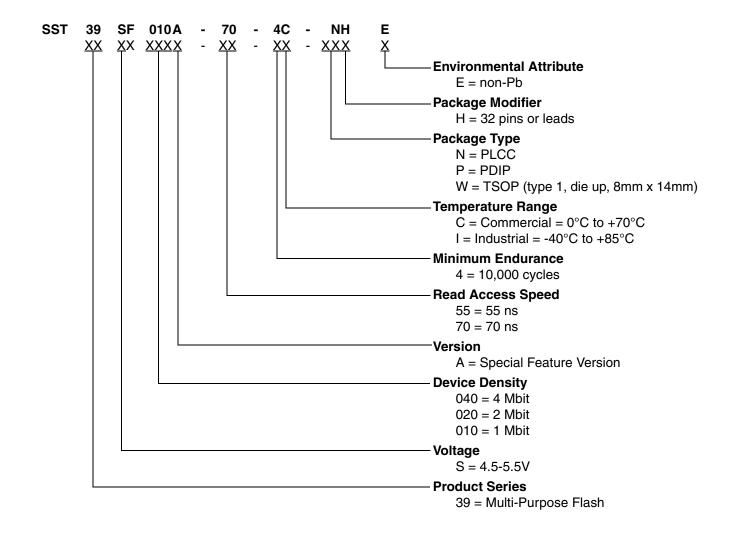


FIGURE 19: Erase Command Sequence



Data Sheet

PRODUCT ORDERING INFORMATION





Valid combinations for SST39SF010A

SST39SF010A-55-4C-NHE	SST39SF010A-55-4C-WHE	
SST39SF010A-70-4C-NHE	SST39SF010A-70-4C-WHE	SST39SF010A-70-4C-PHE
SST39SF010A-55-4I-NHE	SST39SF010A-55-4I-WHE	
SST39SF010A-70-4I-NHE	SST39SF010A-70-4I-WHE	

Valid combinations for SST39SF020A

SST39SF020A-55-4C-NHE	SST39SF020A-55-4C-WHE	
SST39SF020A-70-4C-NHE	SST39SF020A-70-4C-WHE	SST39SF020A-70-4C-PHE
SST39SF020A-55-4I-NHE	SST39SF020A-55-5I-WHE	
SST39SF020A-70-4I-NHE	SST39SF020A-70-4I-WHE	

Valid combinations for SST39SF040

SST39SF040-55-4C-NHE	SST39SF040-55-4C-WHE	
SST39SF040-70-4C-NHE	SST39SF040-70-4C-WHE	SST39SF040-70-4C-PHE
SST39SF040-55-4I-NHE	SST39SF040-55-4I-WHE	
SST39SF040-70-4I-NHE	SST39SF040-70-4I-WHE	

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



Data Sheet

PACKAGING DIAGRAMS

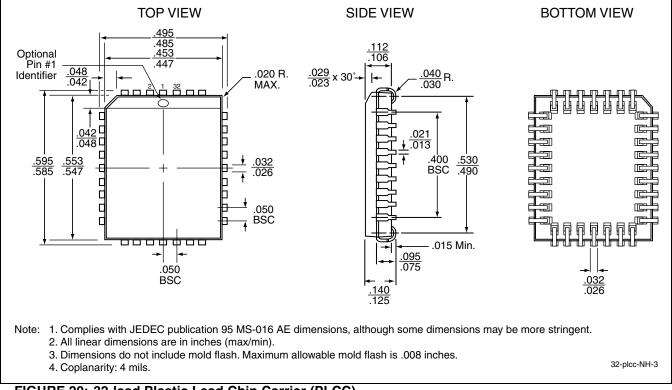
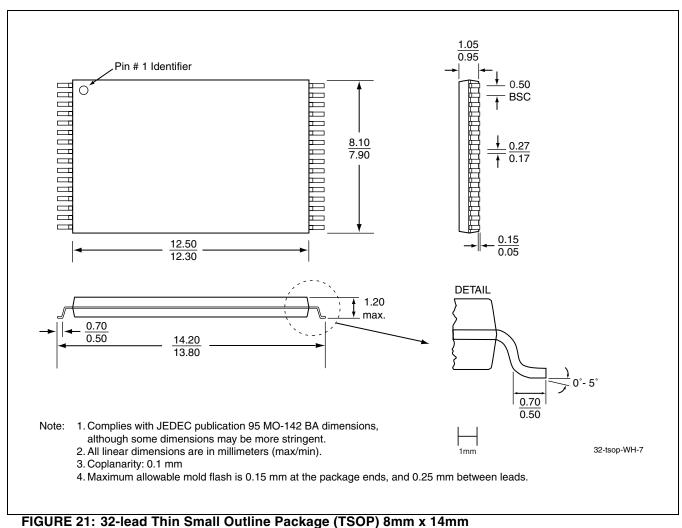


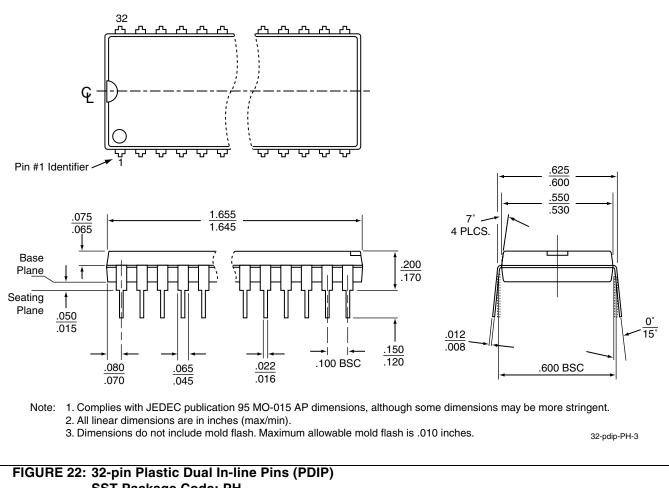
FIGURE 20: 32-lead Plastic Lead Chip Carrier (PLCC) SST Package Code: NH





SST Package Code: WH





SST Package Code: PH



TABLE 11: Revision History

Number	Description	Date
02	2002 Data Book	May 2002
03	Changes to Table 5 on page 8	Mar 2003
	 Added footnote for MPF power usage and Typical conditions Clarified the Test Conditions for Power Supply Current and Read parameters Clarified I_{DD} Write to be Program and Erase 	
04	Document status changed from "Preliminary Specification" to "Data Sheet"	Oct 2003
	Changed I _{DD} Program and Erase max values from 25 to 35 in Table 5 on page 8	
05	2004 Data Book	Nov 2003
	 Added non-Pb MPNs and removed footnote (See page 21) 	
06	 Corrected Revision History for Version 04: I_{DD} max value was incorrectly stated as 30 mA instead of 35 mA 	Aug 2004
07	Removed leaded parts from valid combinations. See PSN-D0PB0001	Mar 2009
08	Changed endurance from 10,000 to 100,000 in Product Description, page 1	Sep 2009
09	• End of Life for all 45 ns valid combinations. See S71147(02).	Jan 2010
	Added replacement 55 ns valid combinations	

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