The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 9916 BUBBLE MEMORY CONTROLLER

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PRELIMINARY

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INCORPORATED

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 9916 is an MOS/LSI implementation of a magnetic-bubble-memory controller (MBMC). The MBMC provides the memory sequencing required to write to and to read from the minor loops of a magnetic-bubble-memory. The MBMC also buffers the bubble data, performs parallel to serial conversion, and maps out any defective minor loops. The TMS 9916 MBMC is fabricated using N-channel silicon gate MOS technology.

1.2 KEY FEATURES

- Compatible with TMS 9900 Microprocessor Families
- Byte-Oriented Transfer of Data
- 20 Bytes of On-Chip Buffer Storage
- Programmable Page Size
- Capable of Ignoring Bad Bubble Loops
- 50-kHz Data-Transfer Clock Rate
- 100-kHz Field Clock Rate
- Two Clocks
- Single-Page or Multiple-Page Modes
- N-Channel Silicon Gate MOS Technology
- General Purpose Memory-Mapped Interface

1.3 TYPICAL APPLICATIONS

Figure 1 illustrates a typical system block diagram. (Refer to Section 3 for a more detailed description of system use.)

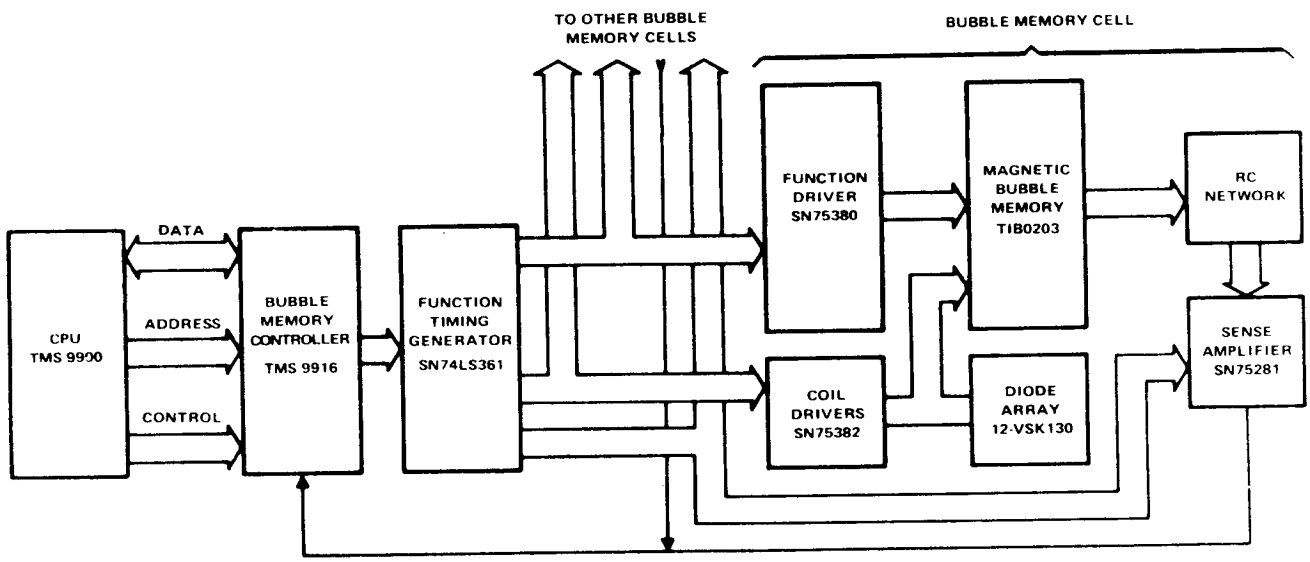


FIGURE 1

1.4 MAGNETIC-BUBBLE MEMORY DESCRIPTION

Small cylindrical magnetic domains, which are called magnetic bubbles, can be formed in single-crystal thin films of synthetic ferrites or garnets when an external magnetic field is applied perpendicularly to the surface of the film. These bubbles can be moved laterally through the film by using a varying magnetic field. These characteristics of magnetic bubbles make them ideally suited for serial storage of data bits; the presence or absence of a bubble in a bit position is used to define the logic state. Since the diameter of a bubble is so small (as little as a tenth of a micrometer), many thousands of data bits can be stored in a single bubble-memory chip. The bubble memory is much like magnetic tape or magnetic disc memory storage in that it is nonvolatile meaning that the data is retained even when power is no longer applied to the chip. Since bubble memories are a product of solid-state technology (there are no moving parts), they have higher reliability than tape or disc storage and do not require any preventive maintenance. In addition, the bubble memory is small and lightweight and is, therefore, an excellent choice for compact designs and portable applications.

1.4.1 Functional Operation Of Bubble Memories

The basic bubble-memory package contains the bubble-memory chip, magnetic field coils, and permanent magnets as shown in Figure 2. A rotating magnetic field created by two mutually perpendicular coils causes the data in the form of magnetic bubbles to move serially through the magnetic film in a manner similar to data in a semiconductor shift register. Two permanent magnets provide nonvolatility and allow for the stable existence of magnetic-bubble domains. Interfacing circuits that are compatible with standard TTL devices complete the memory module to allow a convenient building-block concept for the nonvolatile memory system.

The chip is composed of a nonmagnetic crystaline substrate upon which a thin crystalline magnetic epitaxial film is grown. Only certain materials exhibit the properties necessary to form magnetic bubbles and these include orthoferrites, hexagonal ferrites, synthetic garnets, and amorphous metal films. Among these, the synthetic garnets have the best combination of the desired properties. Synthetic garnets support the formation of small magnetic bubbles that allow high-density data storage. The bubbles are highly mobile and are stable over a fairly wide range of temperatures.

The material chosen for the substrate depends on several factors. The crystalline structure should be compatible with that of the magnetic film, it should have nearly the same coefficient of expansion, and it should be nonmagnetic. The most-used garnet substrate with these properties is gadolinium gallium garnet (GGG). The magnetic film grown on this substrate has a crystalline structure that will allow the formation of magnetic domains (bubbles) in a plane perpendicular to the substrate.

Without the influence of an external magnetic field, these magnetic domains form random serpentine patterns of equal area, minimizing the total magnetic energy of the magnetic film (see Figure 3). The magnetic field of the serpentine domains tends to line up primarily along a single axis (the "easy" axis) that is perpendicular to the plane of the film. If an external magnetic field is applied, its energy tends to expand domains polarized in the direction of the field and to shrink those polarized opposite to the field until they become small cylinders embedded in a background of opposite magnetization. Viewed on end, these cyclinders have the appearance of small circles or bubbles with diameters from 2 to 30 micrometers. Increasing the field further causes the bubble to collapse or to be "annihilated". The external field provides a bias that makes the bubbles stable. This bias, being a static field, can be readily provided by permanent magnets with no expenditure of power.

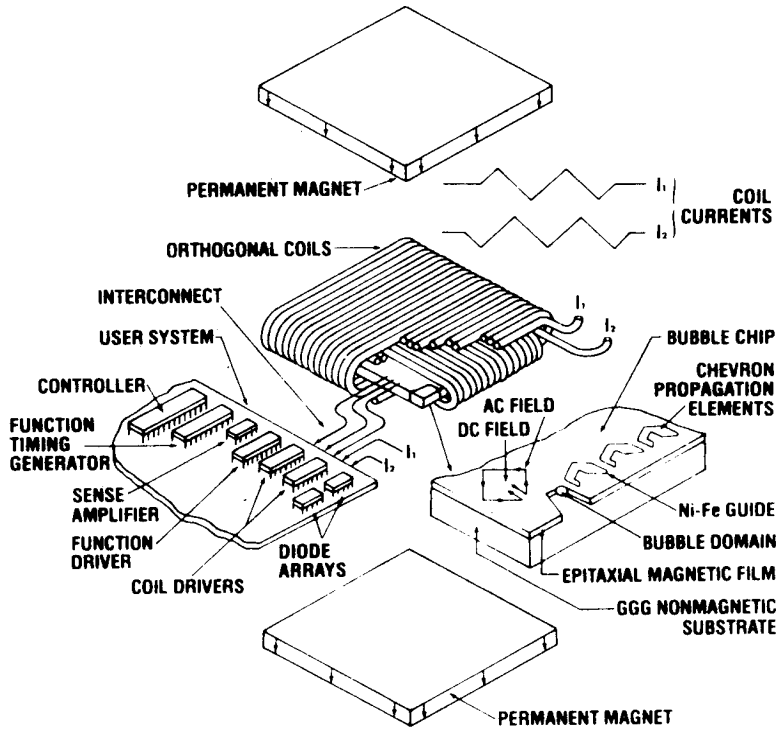
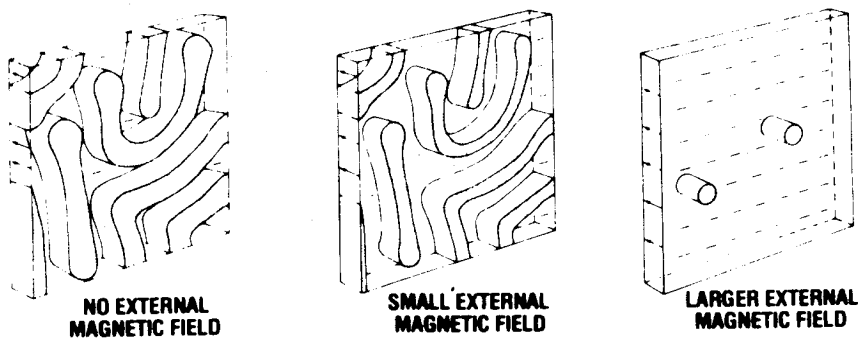


FIGURE 2 – MAGNETIC-BUBBLE MEMORY (EXPLODED VIEW)



External magnetic field shrinks random serpentine domains of magnetically netural crystal to cylindrical form.

FIGURE 3 – MAGNETIC-BUBBLE DOMAINS

Before bubbles can be shifted through the magnetic vilm, they must be generated in accordance with input data. Bubbles are generated by locally altering the bias field with a magnetic field produced by a pulse of current through a microscopic one-turn metallized loop. This loop is located on a secondary layer immediately above the magnetic film on the surface of chip. Given a current of the correct amplitude and polarity through the one-turn loop, a localized vertical magnetic field opposite to that of the permanent magnets is produced. This localized field establishes a domain wall inversion in the magnetic film resulting in bubble creation.

Once a bubble has been created, a method is then required to move the bubble domain along a predetermined path. This is accomplished by the deposition of chevron-shaped patterns of a soft magnetic material on the chip surface above the magnetic epitaxial film. When magnetized sequentially by a magnetic field rotating in the same plane, these chevron propagation patterns set up magnetic polarities that attract the bubble domain and establish motion. Figure 4 shows the various polarities at different positions of the rotating magnetic field. In actual practice the rotating in-plane magnetic field is implemented by applying a two-phase alternating current to the two coils shown in Figure 2.

One possible implementation for the magnetic bubble memory is a long shift register. As shown in Figure 5 the bubbles would shift under the influence of the rotating magnetic field following the path determined by the placement of chevron patterns. Even though this approach offers the simplest design and interface control, it suffers a major disadvantage of having the slowest access time. The reason for this is that after a data bit is entered or written it must circulate through the entire shift register before it can be retrieved or read. Another problem with this single loop design is that a single fault in the shift register structure produces a defective bubble memory chip. This results in a low processing yield and a high cost to the consumer.

For these reasons TI has chosen the major-minor loop architecture, which offers a dramatic improvement in access time. As shown in Figure 6, during a write operation (data entry), data is generated one bit at a time in the major loop. The data is then transferred in parallel to the minor loops where it circulates until the next time data is to be read out of the memory.

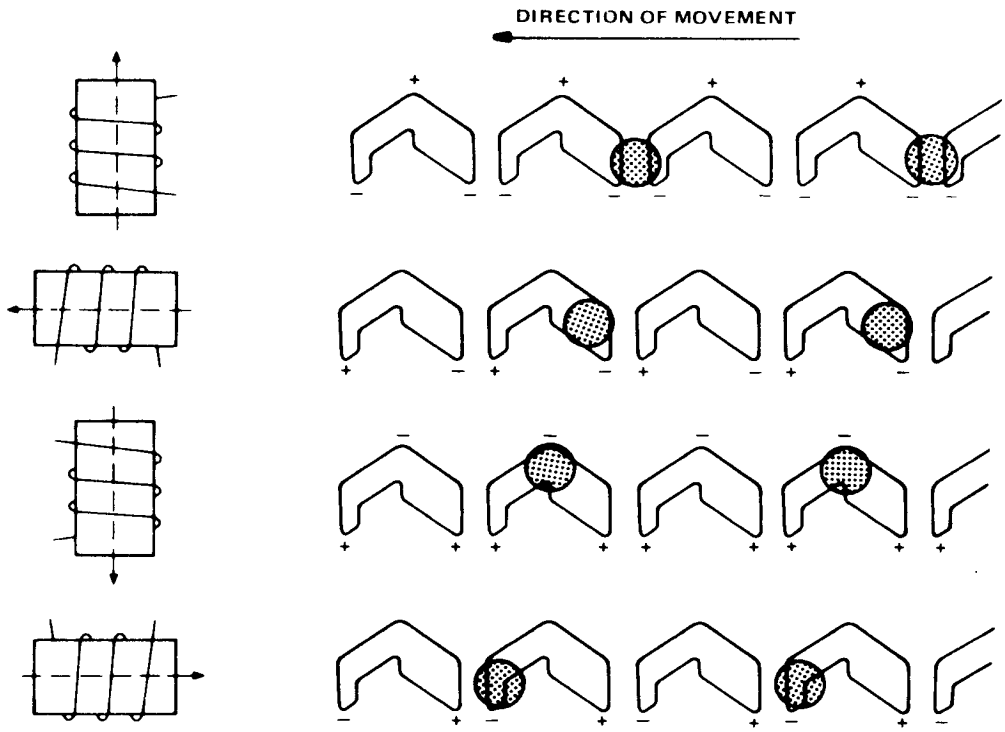


FIGURE 4

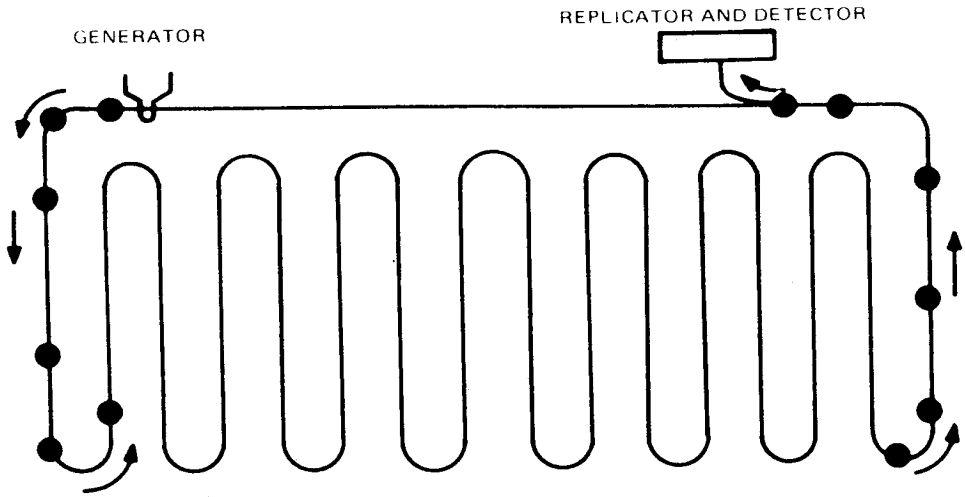


FIGURE 5 – ARCHITECTURE USING A SINGLE LOOP

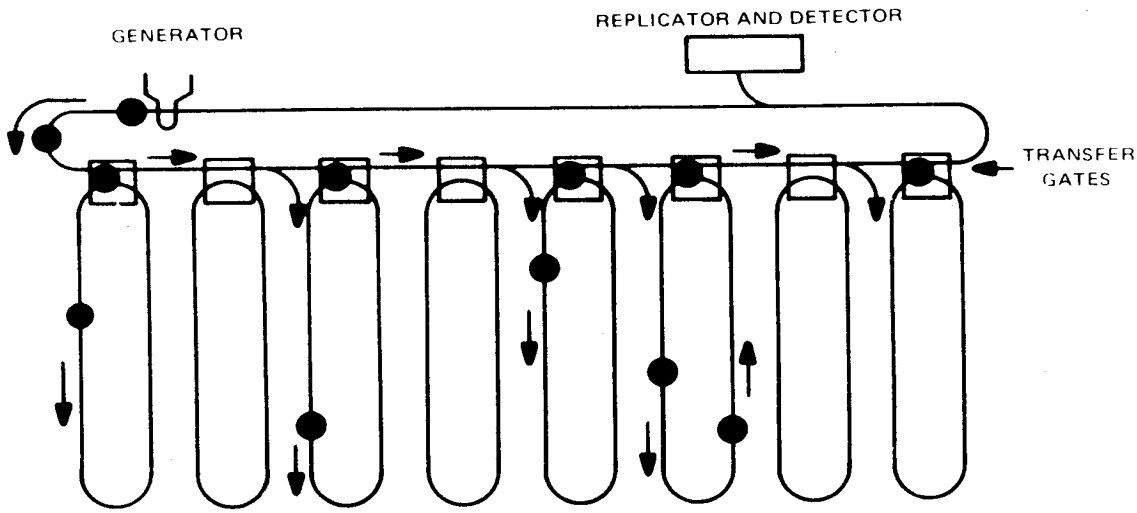


FIGURE 6 – ARCHITECTURE USING MAJOR AND MINOR LOOPS

During a write operation data are introduced into the major loop by pulses of current through the hairpin loop of the generator. The major loop is essentially a unidirectional circular shift register from which data can be transferred in parallel to the minor loops. Thus a block of data is entered in the major loop and shifted until the first data bit is aligned with the most remote minor loop. At that time, each parallel transfer element receives a current pulse that produces a localized magnetic field causing the transfer of all the bubbles in the major loop to the top bit position of the corresponding minor loop. Once data is written into the magnetic bubble memory, new data may be written only by first removing the old data by doing a destructive read. In this operation bubbles are transferred from the minor loops and annihilated.

During a read operation the data block to be accessed in the minor loops is rotated until it is adjacent to the major loop. At this time the data block is transferred in parallel to the major loop. The block of data is then serially shifted to the replicator where the data stream is duplicated. The duplicated data takes the path to the magneto-resistive detector element. The presence of a bubble in the detector lowers the resistance resulting in a corresponding increase in detector current, which can be detected via a sense amplifier. The original data stream remaining in the major loop is rotated and transferred back into the minor loops thus saving the data for further operations.

The magnetic-bubble-memory devices are fabricated using fine geometries that make the manufacture of perfect devices a difficult task. In order to increase production yields and achieve correspondingly lower costs, redundant minor loops on the bubble-memory chip allow some loops to be defective. Defective loops are determined at final test and a map of these loops is supplied to the end user so that the defective loops can be avoided in the final memory system. This redundance of minor loops can be handled in several ways. The map could be written into a software program that would direct data to be stored only to the perfect minor loops, but this would require a unique software package for each memory system. Alternatively, the map could be stored in the MBM (magnetic-bubble memory) itself with some risk of being written over with new data. The recommended approach is to store the map in a programmable read-only memory (PROM). Each bit in a page of data would then be written to the MBM or read from it in accordance with the contents of the PROM, thus preventing data bits from the defective minor loops from mingling with valid data. Of course all this requires control circuitry in addition to that necessary for the timing and control of the alternating current in the field coils, the transfer of data to and from the minor loops, and the replication and detection of the magnetic bubbles.

1.4.2 Advantages Of Bubble Memories

The future growth of distributed process systems will be greatly impacted by magnetic-bubble memories. These microprocessor-based systems demand high-density mass storage at low cost. Magnetic-bubble memories satisfy all of these requirements with definite advantages over the existing magnetic storage technologies. MBM's advantages over moving-head disks or floppy disks are low access time (the time necessary to retrieve the desired data), small physical size, low user entry cost, no maintenance, and higher reliability.

The advantages of MBM's over random-access memories (RAMs) are nonvolatility, potentially lower price per bit, and more bits per chip. The RAM has the advantage of much better access time, higher transfer rate, and simpler interfacing.

In summary, the main MBM advantages are the low entry price versus disks for the low-end user, nonvolatility versus semiconductor memories, and high-density storage in a small physical space. Because magnetic-bubble memories are a solid-state, nonvolatile technology, they are ideally suited for portable applications as well as providing memory for traditional processing systems. Industrial applications include memory for numerical control machines and various types of process control. Solid-state bubble memories are more reliable in harsh environments; they are affected much less by shock, vibration, dirt, and dust then electromechanical magnetic memories. Innovative new products include data terminals, calculators, word processing, voice storage, and measurement equipment.

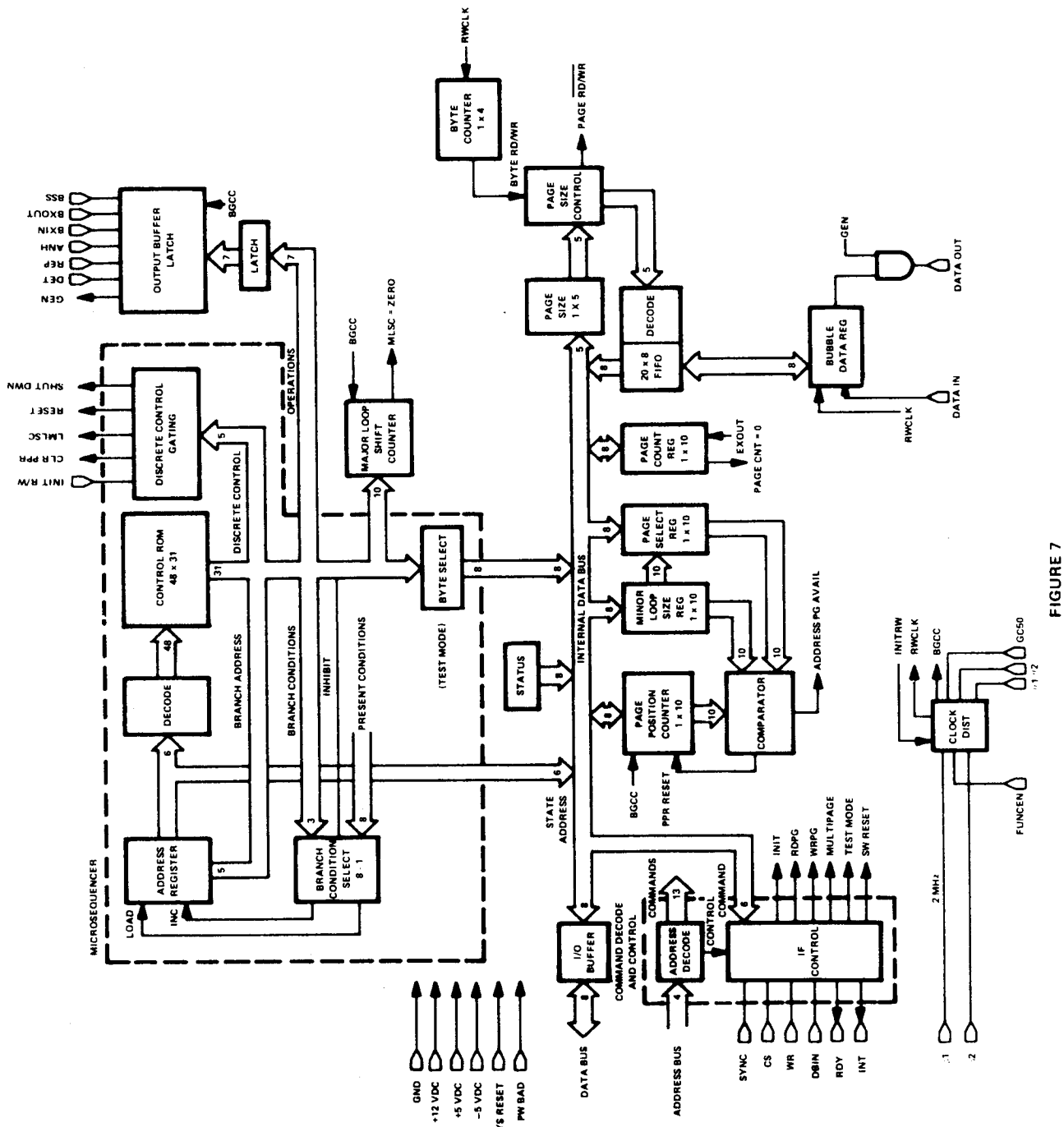


FIGURE 7

1.5 APPLICABLE DOCUMENTS

Texas Instruments	TMS 9980A/TMS 9981 Microprocessor Data Manual
	TMS 9900 Microprocessor Data Manual
	TMS 8080A Microprocessor Data Manaul
	TIB0203 Magnetic-Bubble Memory and Associated Circuits (LCC4430)

2. ARCHITECTURE

Operation is controlled by a microprogram contained in an on-board ROM and by the contents of registers set up during initialization by the programmer. A multiple-page mode is available which enables loading or unloading the memory in blocks of up to the entire contents of memory. A functional block diagram of the TMS 9916 architecture is shown in Figure 7.

2.1 ADDRESS AND CONTROL

The TMS 9916 MBM controller is a Memory-Mapped Device and occupies 16 consecutive locations in memory. Each of the first 15 addresses perform a specific function such as loading a command or loop-size register, reading a status, performing a test, or initiating reading or writing of data. The 16th address (F_{16}) performs no operation. Table 1 lists the addresses and their functions.

The controller executes commands by decoding the four address lines (A0-A3) and gating this decode with either WR or DBIN to form a "read" or "write" strobe ($\overline{WR}$ indicates a write and DBIN indicates a read). Both WR and DBIN are external control signals supplied to the controller. Timing information may be found in Section 4 of this manual.

To provide a convenient interface to the bubble-memory system, a high-level controller is needed to provide read, write, and memory-addressing operations upon command from the user system. The TMS 9916 MBM controller shown in Figure 7 responds to commands from the microprocessor system and enables the necessary control functions to the FTG (function timing generator) to access a page (or pages) of data. The controller maintains page position information, provides internal input/output buffering for one page (160 bits maximum) of data, and handles redundancy by the inclusion of a data inhibit pin which gates out clocks to the internal buffer.

The following is a detailed description of the addressable registers:

ADDRESSABLE REGISTER DEFINITIONS

OPERATION	ADDRESS BITS 0 - 3 DECODE	REGISTER-FUNCTION DESCRIPTION
WRITE	0	Load Page-Select Register 1 (LSB's) Prior to either a read or write page control command, this register must be loaded with the lower 8-bits of the 10-bit address field of the page to be accessed (single-page mode) or the starting page (multipage mode).
WRITE	1	Load Page-Select Register 2 (MSB's) The remaining two MSB's of the 10-bit page-address field must be loaded into the 2 LSB's of this register.
WRITE	2	Load Control Command Register The data loaded into this register indicates specific operations to be done by the controller. (See control section for a detailed description).
READ	3	Read-Byte FROM FIFO
WRITE	4	Write-Byte TO FIFO The internal data buffer* in actuality is a register bank addressed by recirculating pointer. This pointer address is incremented whenever the read-byte or write-byte subaddress is accessed. This pointer must point to the first byte in the buffer before a read or write control command is given. The pointer can be set to the first byte by accessing it the proper number of times or by issuing a system reset.
READ	5	Read Status This register contains continually updated internal status conditions of the controller. (See status bit section for detailed description).
READ/WRITE	6	Page Counter 1 (LSB's)

* Refer to definition of page size register for more details.

OPERATION	ADDRESS BITS 0 - 3 DECODE	REGISTER-FUNCTION DESCRIPTION
READ/WRITE	7	Page Counter 2 (MSB's) In the multipage mode this 10-bit counter must be loaded with the desired number of pages to be transferred by the controller prior to a read or write control command. Once a read or write control command has been initiated in the multipage mode, the controller will decrement the counter at the start of each page transfer. It will continue to transfer data until the page counter reaches a count of zero. In the single page mode the page zero indication from the counter is not used, but the counter is still decremented after each single page transfer. The 8 LSB's are loaded into page counter 1, and the 2 MSB's are loaded into the 2 LSB positions of page counter 2.
WRITE	8	Load Minor Loop Size Register 1 (LSB's)
WRITE	9	Load Minor Loop Size Register 2 (MSB's) This 10-bit register must be loaded once upon power-up of the controller to the hexadecimal value which is equivalent to the number of data positions in the minor loops. In the case of the TIB0203 the value is 0281_{16} which is 641 decimal. The 8 LSB's are loaded into minor loop size register 1. The 2 MSB's are loaded into the 2 LSB positions of minor loop size register 2.
WRITE/READ	A	Page Position Counter 1 (LSB's)
WRITE/READ	B	Page Position Counter 2 (MSB's) This 10-bit counter is used to reference the relative position of data in the minor loops. It actually indicates which page is in position to be transferred into or out of the minor loops. In normal use, upon power-up this counter will be reset to zero. The 8 LSB's are loaded into page position counter 1 and the 2 MSB's are loaded into the 2 LSB positions of page position counter 2. It should not be loaded with any other value. During a read or write page-control-command execution, this counter will be incremented after each 10-microsecond bubble-shift cycle. This counter is internally compared with the page-select register to determine when a transfer-out operation should be done. Upon completion of a data transfer, the controller will continue to rotate the bubble data in the minor loops until the page-position counter reaches reference page-address zero. The page-position counter will modulo-count on one less than the value in the minor-loop-size register. The reference page-address zero can be changed with respect to the data by loading the page-position counter with the absolute value of the displacement in pages minus 641, and executing a read-page control command in the single-page mode.

OPERATION	ADDRESS BITS 0 - 3 DECODE	REGISTER-FUNCTION DESCRIPTION
WRITE	C	Load Page Size Register This register controls the size in bytes of the internal data buffer, which is variable in size from one to 20 bytes. Upon power-up of the controller this register must be loaded to the proper value. In the case of the TIB0203 the value is 12_{16} which is 18 decimal. The data buffer pointer will modulo-count on one less than the value in the page-size register.
READ	D	Read ROM Byte
READ/WRITE	E	Read/Write State Address
UNUSED	F	This register in conjunction with the control command test mode (bit 5) provides no other function than to interrogate the microprogram control ROM in the control section of the TMS 9916. (Used for testing purposes only).

2.2 CONTROL COMMAND REGISTER

Controller commands are decoded and appropriate flags are set which, in turn, signals the microsequencer to begin execution of the control sequences. To minimize pinout on the controller chip, the data bus is used to communicate command information from the external processor. Time reference for this information is furnished by the SYNC, DBIN, and WR signals. Eight bits of data bus, four bits of address, one SYNC line, one DBIN line, one WR line, and one chip select line are supplied to the decode and control unit. The decode and control unit responds with a READY line which ensures completion of an operation before another is initiated. Table 2 lists the commands controlled by the data bits. The control command register is loaded by address 2 (Table 2).

The following is a detailed description of the control command register:

BIT NUMBER	CONTROL BIT DESCRIPTION
0	Initialize When this bit is set, R/S (run/stop) and ANNEN (annihilate-enable) will be turned on for one complete rotation around the major loop to destroy and bubbles that may have for some reason been present in the major loop. This operation need only be performed once after power-up to each bubble cell in the system. The completion time is 6.4 milliseconds. This bit is automatically reset upon completion.
1	Read Page When this bit is set while in the single-page mode, the controller will transfer the page indicated by the page-select register from the bubble module to the controller data buffer. When the data buffer is full (18 bytes), the page read/written status bit will be set. The interrupt line will also be set if bit 7 of the control command register (interrupt-inhibit) has not been previously set when the read command was given. At this time the 18 bytes of data may be read out consecutively via the read byte subaddress register. Reading the data will reset the page read/written bit and the interrupt. Another control command cannot be issued until the controller-busy status bit makes a one-to-zero transition. To operate the TMS 9916 in the multipage mode, provisions must be made to operate in an interrupt driven capacity or to externally test the interrupt driven capacity or to externally test the interrupt output (pin 34) of the controller. Before

BIT NUMBER	CONTROL BIT DESCRIPTION
	initiating the multipage read command, the page-count registers must first be loaded to the desired number of pages to be transferred. Then the page-select registers must be loaded to the desired starting page. (It should be kept in mind that when in a multipage block transfer mode the pages of data are not accessed sequentially but are a constant 322 positions apart for the TIB0203. For example, if 4 pages are transferred starting at page zero, these pages will be accessed as follows: 0;322;4;326;. When the control-command word is loaded to initiate the transfer, the multipage mode bit* must have previously been set and the interrupt must not be inhibited). When in multipage mode the FIFO becomes a single byte buffer, which necessitates the microprocessor access the read-byte register once after each interrupt. An interrupt will be issued every 160 microseconds corresponding to each byte transferred. The act of reading the data buffer will reset the interrupt. By interrogating the page-count zero status bit after each interrupt, the microprocessor can determine when the last page is being transferred. Another control command cannot be issued until the controller-busy status bit makes a one-to-zero transition.
2	Write Page The write-page command process is similar in detail to the read-page command except that the interrupt is set when the data buffer is empty. When operating in the interrupt driven mode, the inhibit-interrupt control-command bit must be set after the last byte has been transferred in order to reset the interrupt line. This applies to both multipage and single-page mode. Also the data buffer must be loaded before initiating a write operation. In single-page mode, cycles are approximately 12.8 milliseconds. The multipage transaction time equals 6.41 milliseconds plus the number of pages to be transferred times 3.22 milliseconds.
3	Single-Page Mode This bit sets the controller to the single-page mode. This bit is also set by system-reset, but once it is set, it is not necessary to set it again. It will only be reset by setting the multipage bit.
4	Multipage Mode This bit sets the controller to the multipage mode. It should be set prior to initiating a multipage write or read. It need only be set once unless a system reset occurs or single-page mode is set.
5	Reserved
6	Reset This bit allows the reset function to be done via software. This does not reset FIFO pointer.
7	Interrupt-Inhibit When this bit is set the interrupt to the microprocessor is inhibited. If the interrupt-inhibit command is set during a read or write operation, it will inhibit the interrupt from being issued for the balance of the transfer. It will also reset an interrupt currently being issued.

* For more detail see description of multipage mode bit.

2.3 STATUS REGISTER

Controller status is maintained in this register and can be read by the microprocessor. Table 3 lists these status conditions. Address 5 is used to read the status register.

The following is a detailed description of the status register:

BIT NUMBER	STATUS BIT DESCRIPTION
0	Page Read/Written In the single-page mode this bit will be set when the transfer of data to or from the FIFO data-buffer is complete. It will be reset by a status-read operation.
1	Reserved
2	Reserved
3	Major-Loop Shift-Counter Equal to Zero A logic one indicates the major-loop shift-counter (MLSC) has reached address zero. It is reset by a status-read operation. (Used for testing purposed only).
4	Addressed-Page Available This bit is set whenever the page-select register and the page-position counter become equal. It is reset upon a status-read operation.
5	Controller Busy A logic one indicates that the controller is in the process of transferring data to or from the bubble memory. Another control command should not be issued until the busy bit makes a one-to-zero transition. Approximately 10 microseconds elapse before controller-busy is indicated after issuing the controller a control command during initialize, write, or read operations. Therefore it is necessary to wait until controller-busy is indicated and then test for controller-not-busy.
6	Page-Count Equal to Zero This bit is set whenever the page-count register is decremented to zero. It will be reset when the page-count register is reloaded.

NOTE: Since many of the status bits are reset when the status register is read, no conflict will occur in setting and resetting the bits (i.e., the bit is set on a different clock phase then it is reset).

BIT NUMBER	STATUS BIT DESCRIPTION
7	Byte Read/Written In the multipage read mode, this bit indicates that the FIFO buffer has been loaded with a byte of data and is ready for reading by the microprocessor. In the multipage write mode, this bit indicates that the FIFO buffer has been transferred to the bubble data register and is ready to accept new data from the microprocessor. Byte RD/WR will be set every 160 μs (minimum). The status bit is reset when status is ready by the microprocessor.

NOTE: Since many of the status bits are reset when the status register is read, no conflict will occur in setting and resetting the bits (i.e., the bit is set on a different clock phase then it is reset).

TABLE 1 – ADDRESS FUNCTIONS

ADDRESSES (A0-A3)	DATA COMMANDS	OPERATION
0	Load Page Select Reg 1	Write LSB
1	Load Page Select Reg 2	Write MSB
2	Load Control Command Register	Write (see Table 2)
3	Read Byte	Read FIFO
4	Write Byte	Write FIFO
5	Read Status	Read
6	Page Counter 1	Read/Write LSB
7	Page Counter 2	Read/Write MSB
8	Load Minor Loop Size Reg 1	Write LSB
9	Load Minor Loop Size Reg 2	Write MSB
A	Page Position Counter 1	Read/Write LSB
B	Page Position Counter 2	Read/Write MSB
C	Load Page Size Reg	Write
D	Read ROM Byte (for testing only)	Read & Incr. Pointer
E	Read/Write State Address (for testing)	Read ROM ADDR Reg

NOTE: Address decode F will cause no action by the controller.

TABLE 2 – CONTROL COMMAND BIT DEFINITION

BIT NO.	CONTROL COMMAND	RESET FUNCTION	FUNCTION
0	Initialize	System* + CRRST**	"Cold Start" initialization
1	Read Page	System + CRRST	Read page from bubble memory into FIFO page buffer
2	Write Page	System + CRRST	Write page from FIFO page buffer into bubble memory
3	Single Page Mode	Bit 4 = "1"	Sets up controller for single page transfers
4	Multi-Page Mode	System + Bit 3 = "1"	Sets up controller for multi-page transfers
5	Reserved	System + Bit 5 = "0"	
6	Reset		Software System Reset (Pulse)
7	Interrupt Mask	System + Bit 5 = "0"	Resets Interrupt Level (Pulse)

* System = software reset + hardware reset
** CRRST is a discrete control bit in the control ROM

TABLE 3 – STATUS CONDITIONS

BIT	CONDITION	SET FUNCTION	RESET FUNCTION
0 (LSB)	Page Read/Written	Page Size Counter	Status Read SRST
1	Load/INCR	Updated on State Transition	
2	Inhibit	Updated on State Transition	
3	MLSC Zero	Major Loop Shift Counter = 0	Status Read SRST
4	Addressed Page Available	Comparator	Status Read SRST
5	Controller Busy	Leaving State 0	1 to 0 transition of BSS
6	Page Count Zero	Page Count Register	Page Count Register Loaded
7 (MSB)	Byte Read/Written	Byte Counter	Status Read SRST

2.4 PAGE-POSITION COUNTER (PPC)

The page-position counter is the bubble memory address mechanism. BGCC (see Section 2.14), the 100-kHz bubble-memory-gated shift clock, is connected directly to the PPC to ensure absolute tracking of page position. Ten (10) bits are required to meet block sizes up to 1023 pages. This register can be read or written from the microprocessor using addresses A_{16} and B_{16} for the LSB's and MSB's, respectively. Address A_{16} loads the eight LSB's of the PPC from the data lines while address B_{16} loads the two MSB's of the PPC from the two LSB's of the data lines.

2.5 PAGE-SELECT REGISTER (PSEL)

Pages of memory are addressed by insertion of the desired page number into the page-select register. This 10-bit register is compared with the page-position counter to determine when the addressed page is available. Controller addresses 0 and 1 are used for loading this register. Address 0 loads the eight LSB's of the PSEL from the data lines while address 1 loads the two MSB's of the PSEL from the two LSB's of the data lines.

2.6 MINOR-LOOP-SIZE REGISTER (MLSR)

The MLSR is a 10-bit register loaded as function of the bubble chip used with the controller. This register determines the reset point of the page-position counter. This register needs to be loaded only on initialization. Address 8 controls the eight LSB's and address 9 controls the two MSB's.

2.7 PAGE-COUNT REGISTER (PCR)

This counter/register is used in conjuction with multipage transfers to hold the desired block size to be transferred under a read-page or write-page command. Block transfers up to 1023 pages may be handled with this 10-bit counter. For single-page transfers, a read-page or write-page control command is executed with the controller set to the single-page mode. (NOTE: single-page mode overrides the PCR.) This counter is decremented on each INTRW for both single-page and multipage modes.

2.8 PAGE-SIZE REGISTER (PSR)

Various page sizes, in bytes, up to 20 bytes may be handled by the bus structure and other registers. This five-bit displacement is loaded under microprocessor control and is a function of the bubble chip used with the controller. The page-size register needs to be initialized only during the power-up sequence. Address C_{16} is used for this register. The five LSB's of the data lines are loaded into the PSR.

2.9 PAGE BUFFER

Up to 20 data bytes may be stored in this first-in-first-out (FIFO) page buffer. In the single-page mode data is written into the page buffer one byte at a time, and when it is full, a write-page control command unloads a full page to the bubble memory. Similarly, on read operations a full page is read from memory into the FIFO and subsequent read byte commands unpack the data. A byte pointer is maintained to facilitate minimum overhead in accessing the page buffer. A system reset will reinitialize the FIFO pointer to point to the first FIFO byte. On multipage transfers, only one byte of the buffer is utilized. Status conditions (byte RD/WR, page RD/WR) and interrupts indicate when this buffer can be read or written. Addresses 3 and 4 are used to read and write, respectively, a byte of data.

2.10 PAGE SIZE COUNTER

This five-bit counter is loaded by the controller from the page-size register and counted down to zero with the byte RD/WR signal. The zero count indicates that the controller has written or read a page of data (page RD/WR) from the bubble module. The page RD/WR signals goes to the status register and to the controller interrupt logic. The page-size counter is automatically reloaded after it has reached a count of zero. (NOTE: When the page size register is loaded from the microprocessor, this counter is also loaded.) Upon writing a page to or reading a page from the FIFO, the page RD/WR status bit will be set. This counter serves as a pointer for bytes in the FIFO buffer.

2.11 BUBBLE DATA REGISTER (BDR)

Data bytes are transferred in and out of the BDR using the 50-kHz read/write clock (RWCLK). Parallel-to-serial conversion is accomplished through the eight-bit BDR for data transfers with the bubble memory. Serial shifting of the data stream is accomplished in conjunction with RWCLK clock to synchronize the read/write operation.

2.12 BYTE COUNTER

The byte counter is a three-bit counter used to determine when eight good bits of data have been shifted into or out of the bubble data register. After eight data bits have been transferred, the byte RD/WR signal is generated and used to set a status bit, generate an interrupt (multipage mode), and to decrement the page-size counter. The RWCLK which clocks the byte counter is gated with an external function-enable (FUNCEN) signal to allow the controller to ignore bad incoming data bits.

2.13 MICROSEQUENCER

The microsequencer is basically a simplified synchronous sequential machine whose states are distinct memory locations in the control ROM. As a state machine the microsequencer can move to one of three states from any present state: the same state, the next sequential state, or a branch to any other state. The output-buffer latch is controlled by the microsequencer. From this latch come the control for the bubble-memory function-timing generator.

2.14 CLOCK DISTRIBUTION

All controller timing is derived from the 2-MHz two-phase ($\phi 1, \phi 2$) system clock. The 2-MHz clock is divided down to generate two other phases ($\theta 1, \theta 2$) which are 100 kHz and 90 degrees out of phase $\theta 1$ is gated with the bubble-start-shift signal (BSS) from the microsequencer to generate the bubble-memory-gated shift clock (BGCC). $\theta 1$ and $\theta 2$ are available on external pins. BGCC is used internally to the controller. A 50-kHz clock (GC50), also available on an external pin, represents the data rate in the major loop (half the rate of the minor loops).

Data is shifted into and out of the controller serially with a 50-kHz read/write clock (RWCLK). This clock is gated with an external function-enable (FUNCEN) signal which forces the controller to ignore bad loops in the bubble memory. For perfect chips FUNCEN would be tied to a logic one level. NOTE: A transfer operation to/from the controller can not begin until 15 ϕ clock cycles after RSET becomes inactive (low).

2.15 BUBBLE-MEMORY SYSTEM TIMING REQUIREMENTS

The function timing generator (FTG) integrated circuit provides input-timing control to the function driver, coil drivers, and sense amplifier on a per-cycle basis. Control signals are provided to the input of the function driver to provide five basic operations: generate, replicate, annihilate, transfer in, and transfer out. The control signals to the coil drivers handle start/stop operation and also maintain the 90-degree phase relationship between the two coils in the MBM. The sense amplifier receives a control input for an internal-ac restore circuit and a strobe input to clock the detected data into an internal D flip-flop. The FTG contains internal voltage sensing that places its output into a high-impedance state when the positive 5-volt supply falls below a prescribed level. The function driver and coil drivers are designed to detect the high impedance state in order to inhibit their respective output stages during power up/down conditions. The FTG output stages are designed to drive up to 17 MBM devices and their respective interface circuits. To drive more than 17 MBM subsets, a buffer must be used that contains the internal voltage sensing which in turn provides the high-impedance state when the supply voltage is in a transition state.

2.16 BUBBLE MEMORY INTERFACE REQUIREMENTS

Since the MBM requires accurate current pulses for the generate, replicate, and transfer elements, an interface circuit (function driver) is needed for the conversion from digital input control signals. Also, the MBM has two internal coils which each require a triangular current drive 90 degrees out of phase with the other coil. This requirement is satisified with another set of interface circuits (coil drivers and diode array) driven with digital input signals. The net loaded peak output signal amplitude of the MBM is typically 3 millivolts. To be useful in a system, the output is converted to digital levels with the use of a set of interface circuits (R/C network and sense amplifier) that set up detector biasing and provide a sensitive level sensing circuit whose output is stored in an internal D flip-flop. In summary, the following interface integrated circuits are required on a recurring basis for each MBM in a system: one function driver, two coil drivers, one diode array, one R/C network, and one sense amplifier. To use the TMS 9916 with the chevron version of the 92K bubble memory, it is necessary to delay the transfer-in enable output (BXIN) by one bubble-field cycle. This is necessary because there is one position in the major loop of the TIB0203 (chevron) bubble memory than in the earlier TIB0103 T-bar version of the 92K bubble memory device.

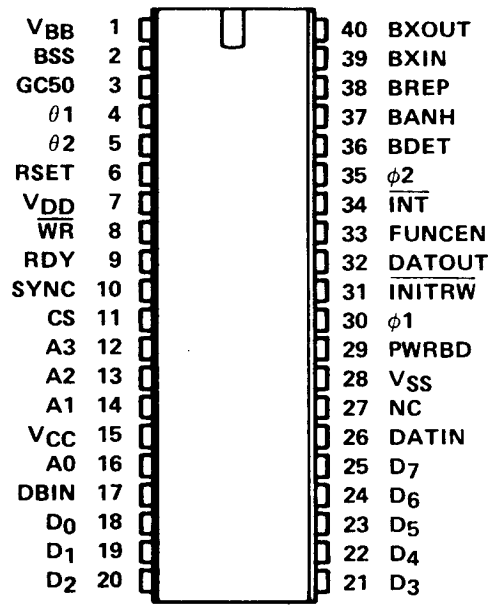
2.17 TMS 9916 TERMINAL ASSIGNMENT

Table 4 defines the TMS 9916 terminal assignments and describes the function of each terminal.

TABLE 4. TERMINAL ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
V_{BB}	1	I	−5 volt supply
BSS	2	O	Bubble start shift, used to start and stop bubble-field drive clocks.
GC50	3	O	Gated 50-kHz clock synchronous with the data transfer rate out of the bubble module.
$\theta 1$	4	O	Timing signals to the function timer.
$\theta 2$	5	O	
RSET	6	I	Initialization signal which resets the following functions: 1) Status register (except page count zero, which is set) 2) ROM function latch 3) Byte counter 4) Interrupt 5) Output Buffer 6) Control signals 7) ROM address register 8) Flags — multipage, initialize, read page, write page 9) Page-count register 10) Page-select register 11) Byte select 12) Clock distribution
V_{DD}	7	I	+12 volt supply voltage
$\overline{WR}$	8	I	Write signal to the controller indicating that the processor is executing a write instruction.
RDY	9	O	Signal generated by the controller that indicates the controller is ready for a new bus transfer.
SYNC	10	I	Synchronization signal to the controller indicating that a command sequence is starting (see Note 2).
CS	11	I	Chip select to the controller which enables the command decode logic.
A3 (MSB)	12	I	Four address lines used for encoding commands to the controller.
A2	13	I	
A1	14	I	
A0 (LSB)	16	I	
V_{CC}	15	I	+5 volt supply
DBIN	17	I	Data-bus-in signal to the controller, indicating the processor is executing a read instruction.
D0 (LSB)	18		
D1	19		

TMS 9916 ASSIGNMENTS



SIGNATURE	PIN	I/O	DESCRIPTION
D2	20		
D3	21		
D4	22		
D5	23		
D6	24		
D7 (MSB)	25	I/O	Data is transferred to and from the processor over this bidirectional data bus.
DATIN	26	I	Serial data from the bubble module to the controller.
	27		No connection
V_{SS}	28	I	Ground
PWRBAD	29	I	Power-bad signal to the controller indicating that the power source has been interrupted and an orderly shutdown should be initiated. This permits the controller to circulate the memory to its zero address, for a known starting point on power up.
$\phi 1$	30	I	Two-phase 2-MHz clock which governs all of the controller timing sequences
$\phi 2$	35	I	
$\overline{\text{INITRW}}$	31	O	Initiate read-write signal from the controller indicating that it is about to read or write from to the bubble module.
DATOUT	32	O	Serial data from the controller to the bubble module.
FUNCEN	33	I	Function enable to the controller, generated by the PROM used to inhibit data shifting when there is a bad minor loop in the bubble memory.
$\overline{\text{INT}}$	34	O	Interrupt signal generated by the controller to the processor indicating data is ready to be read or written.
BDET	36	O	Bubble-detect enable signal indicates that a page of bubbles is passing the detector and should be read.
BANH	37	O	Bubble-annihilate signal from the controller, indicating that bubbles in the annihilate position in the major loop should be collapsed (see Note 1).
BREP	38	O	Bubble-replicate signal from the controller indicating that the bubble located at the replicate position in the major loop should be split into two bubbles. One continues along the major loop, the other travels towards the detector (see Note 1).
BXIN	39	O	Transfer-in enable, indicating that bubbles in the major loop are to be transferred to the minor loops (see Note 1).
BXOUT	40	O	Transfer-out enable indicating that bubbles in the minor loops are to be transferred to the major-loops (see Note 1).

NOTES: 1. Transfer of a bubble between major and minor loops, and from major loop to read area is a destructive process, that is the bubble transferred is "annihilated". The replicate signal enables the bubble to be split as it heads for the read area, so that it can continue around the major loop, eventually to be restored to its proper position in a minor loop.

2. In applications where a separate SYNC signal is not available, SYNC and CS may be tied together.

3. DEVICE APPLICATION

This section describes the hardware and software interface between the CPU, Bubble Memory and the TMS 9916 MBMC.

Since the magnetic-bubble memory requires accurate current pulses for the generate, replicate, and transfer operations, an interface circuit called a function driver is needed to convert the digital input control signals to the required current pulses. Also, the two field coils each require a triangular current drive 90 degrees out of phase with each other. This requirement is satisfied with another set of interface circuits (coil drivers and diode array) that is driven with digital input signals. The output signal amplitude of the MBM is relatively small, about 3 millivolts. For this to be useful in a system, the output is converted to standard TTL levels with the use of a set of interface circuits (RC networks and sense amplifiers). The block diagram in Figure 8 shows the connection of all these interface circuits as a memory module. This modular building block promotes efficient construction of mass memories.

The control and timing signals for the memory module are derived from the function-timing generator. This integrated circuit provides input timing control to the function driver, coil drivers, and sense amplifier on a per-cycle basis. The function-timing generator provides control signals to the memory module as shown in Figure 9. These signals provide control for five basic operations: generate, replicate, annihilate, transfer-in, and transfer-out. The function-timing generator also initiates the rotating magnetic field and precisely synchronizes the timing of other control signals with this field.

The time at which a particular data bit is detected in the MBM may not exactly match the time at which it is needed in the system. The sense amplifier not only increases the voltage level of the detected data, but also provides temporary storage of the data bits in a circuit called a D-type flip-flop. The sense amplifier receives a control input from the function timing generator to transfer the detected data into the internal flip-flop. In addition, the function-timing generator provides the control signals necessary to put the existing data in a known position during a power shut down. When the system is turned on again, the stored data can then be accurately located and retrieved.

In a typical system the major computing and data processing is done by a microprocessor. To provide a convenient interface from the microprocessor to the MBM system, a custom controller is needed for the read, write, and memory-addressing operations. The TMS 9916 MBM controller responds to commands from the microprocessor system and sends control signals to the function timing generator necessary to access a page (or pages) of data. The controller maintains page-position information, handles serial-parallel data conversion between the bubble memory and the microprocessor, and generates the control signals to the function-timing generator to perform read and write operations while handling the redundancy of the minor loops.

3.1 USE OF THE TMS 9916 WITH THE TMS 9980

The TMS 9980 microprocessor is designed to read or write two bytes of data at a time. To interface the TMS 9916 (which is a single-byte peripheral) to the TMS 9980, the TMS 9916 must occupy only odd bytes. This is done by moving up one bit in significance each of the address lines to the controller and decoding the least significant bit as a logic one. WE and DBIN must be gated with the chip-select signal to avoid improper control signals.

3.2 TMS 9900 INTERFACE

A typical application of a TMS 9900 to a TMS 9916 is shown in Figure 10.

3.3 TMS 9916 INTERFACE WITH BUBBLE MEMORY

A typical application of a TMS 9916 to a Bubble Memory and associated circuits is shown in Figure 10.

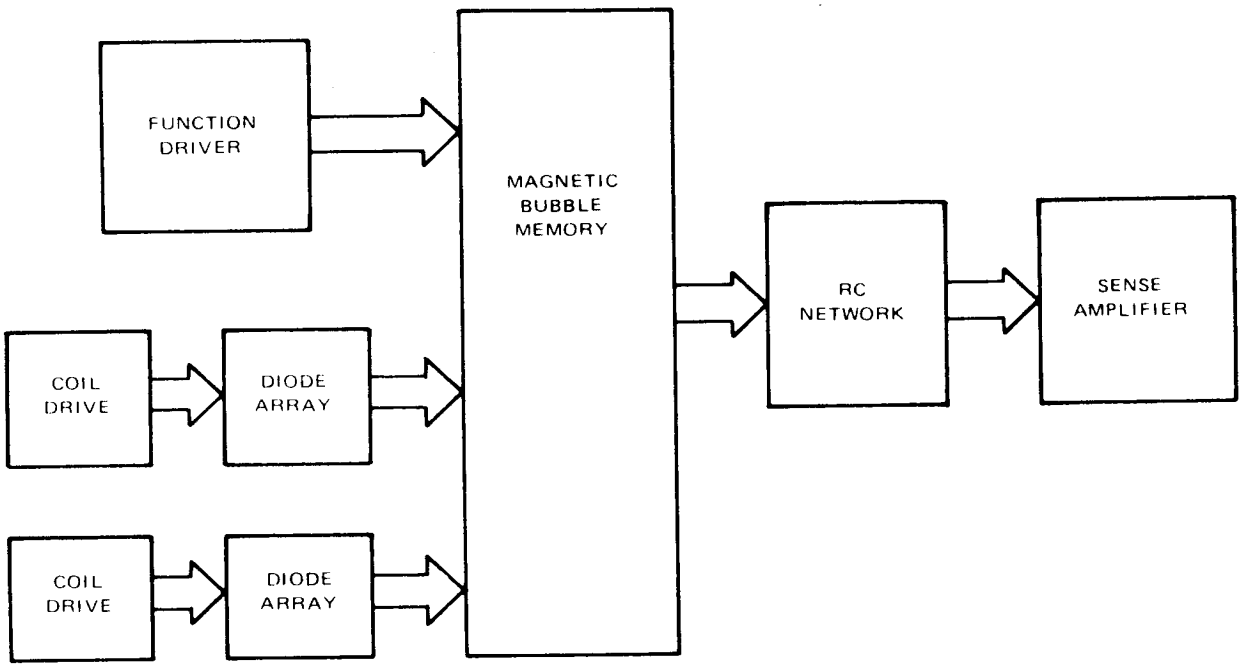


FIGURE 8 – BUBBLE MEMORY MODULE

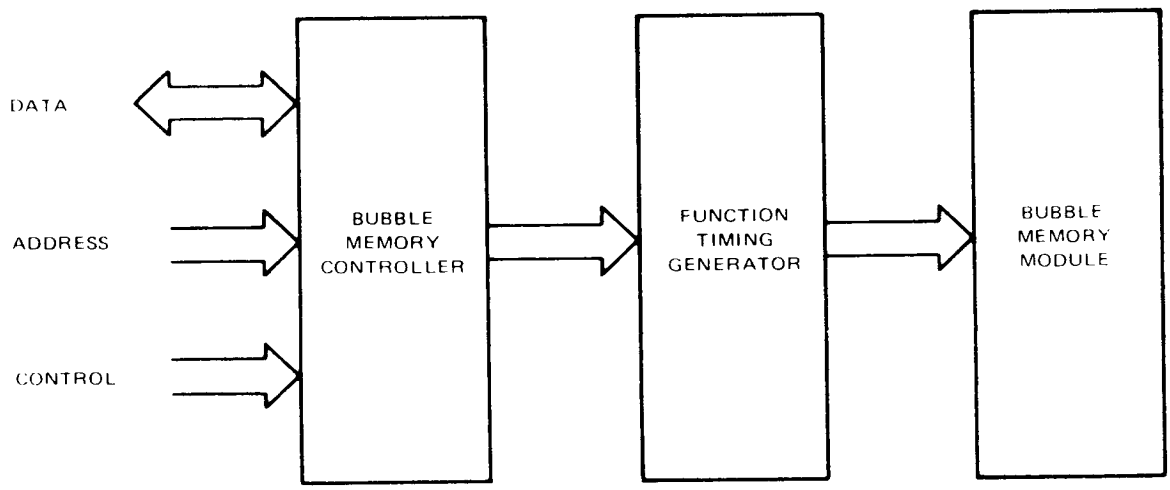


FIGURE 9 – TIMING AND CONTROL FUNCTIONS

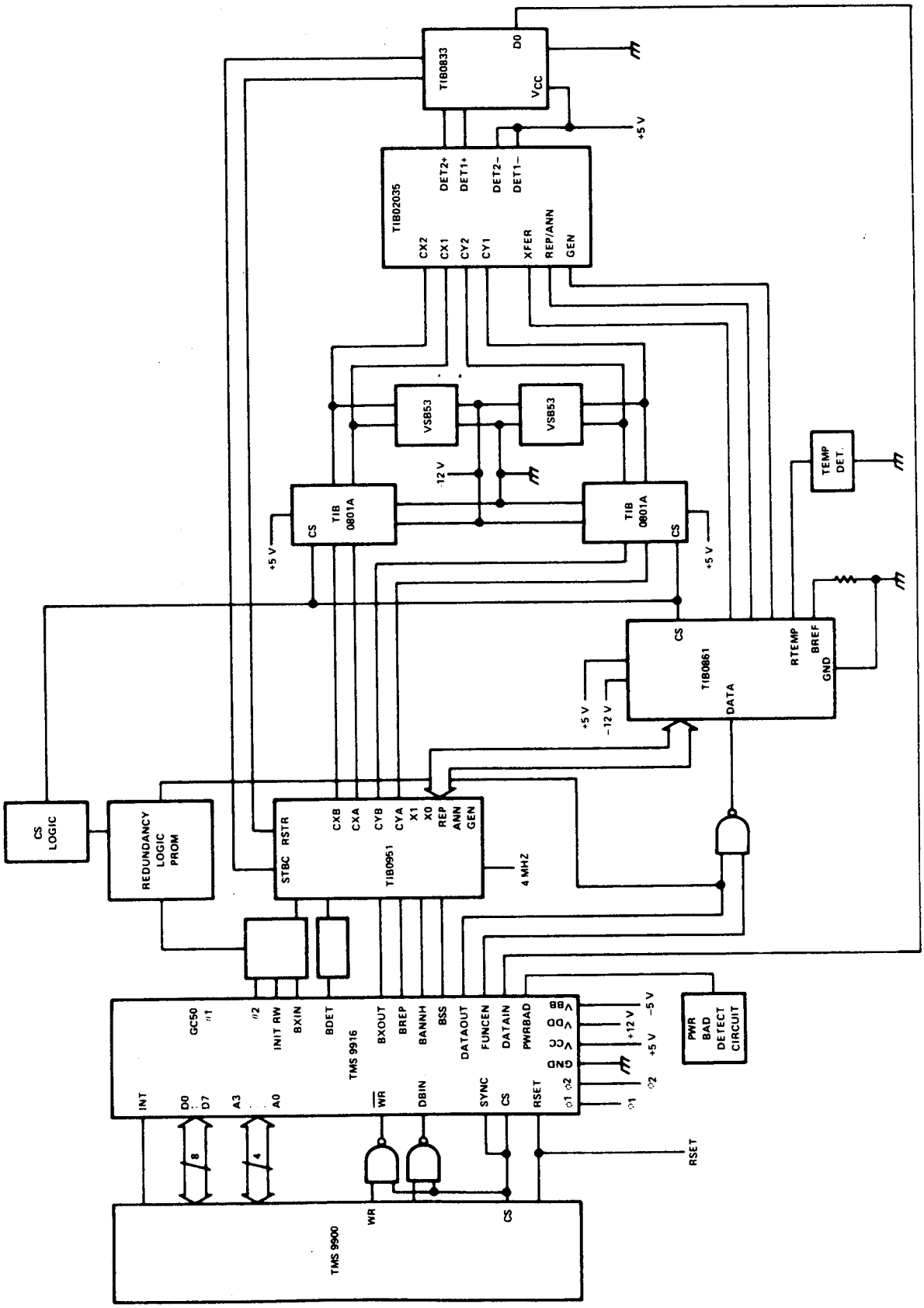
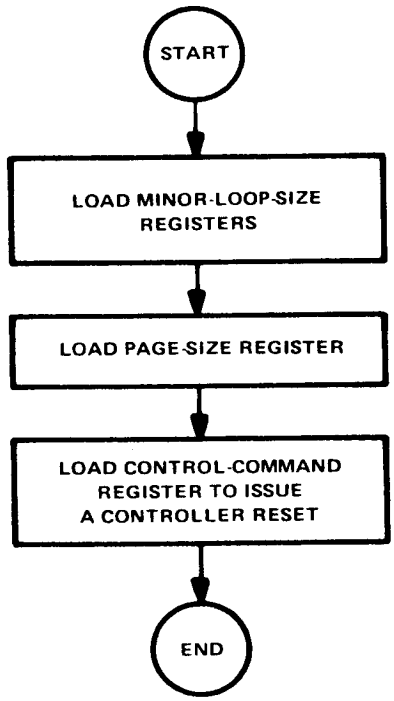


FIGURE 10 – TMS 9900-TO-TMS 9916-TO-BUBBLE MEMORY INTERFACE

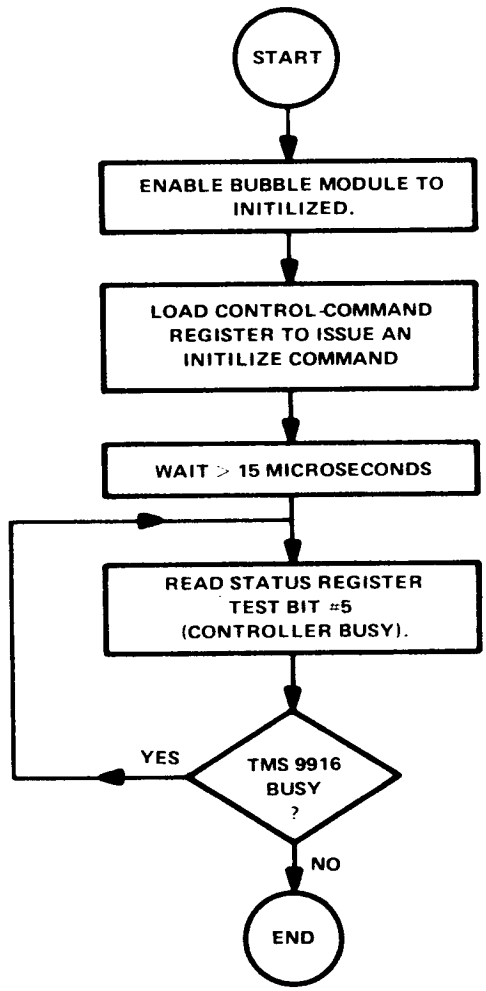
3.4 TMS 9916 SOFTWARE INTERFACING FLOWCHARTS

These flowcharts are to be used when interfacing the magnetic-bubble-memory controller to a microprocessor. The controller power-up initialization needs to be done once after power-up to load the minor-loop size. The bubble memory power-up initialization needs to be done separately for each bubble memory to annihilate any bubbles in the major loop.

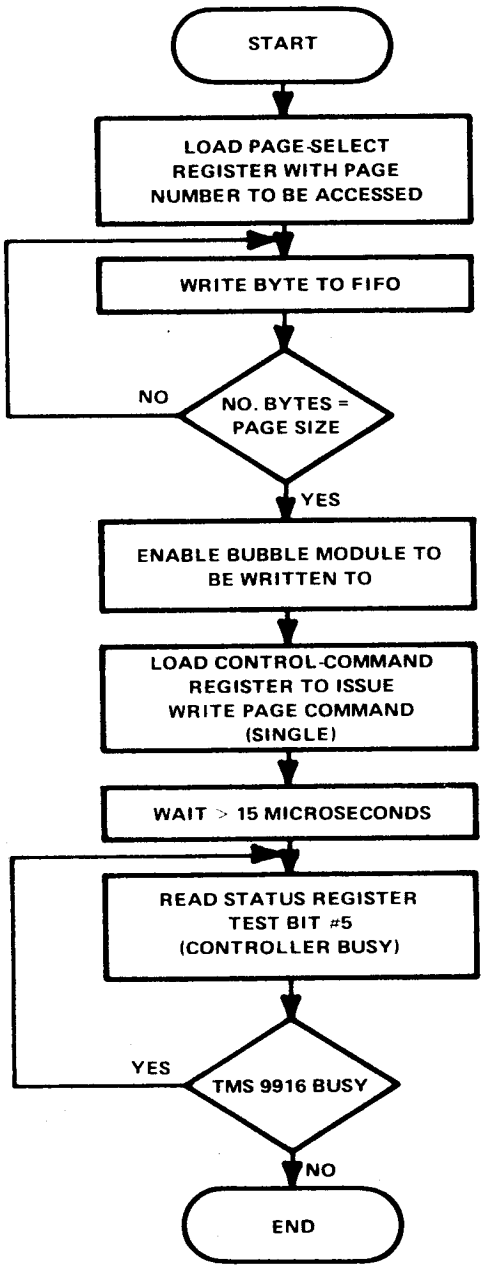
CONTROLLER POWER UP INITIALIZATION



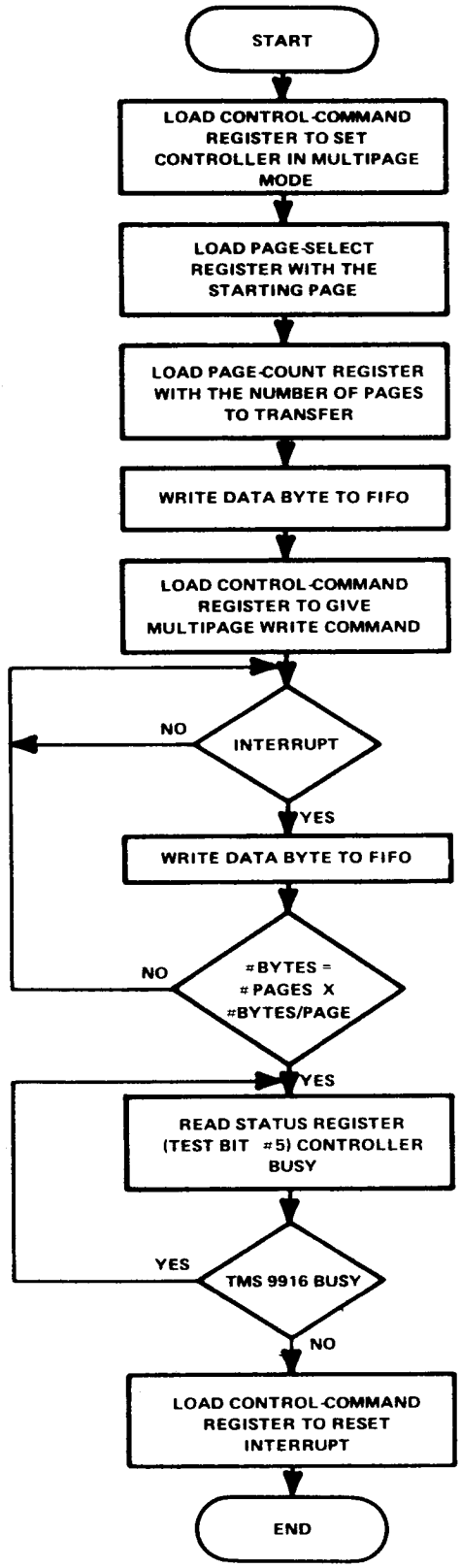
BUBBLE MEMORY POWER UP INITILIZATION

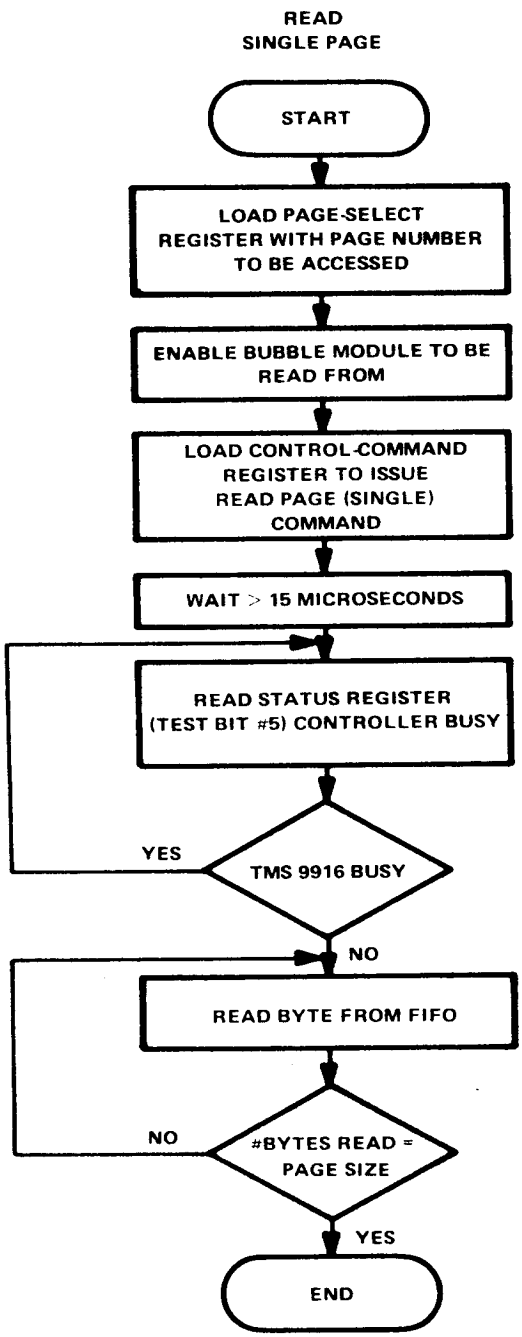


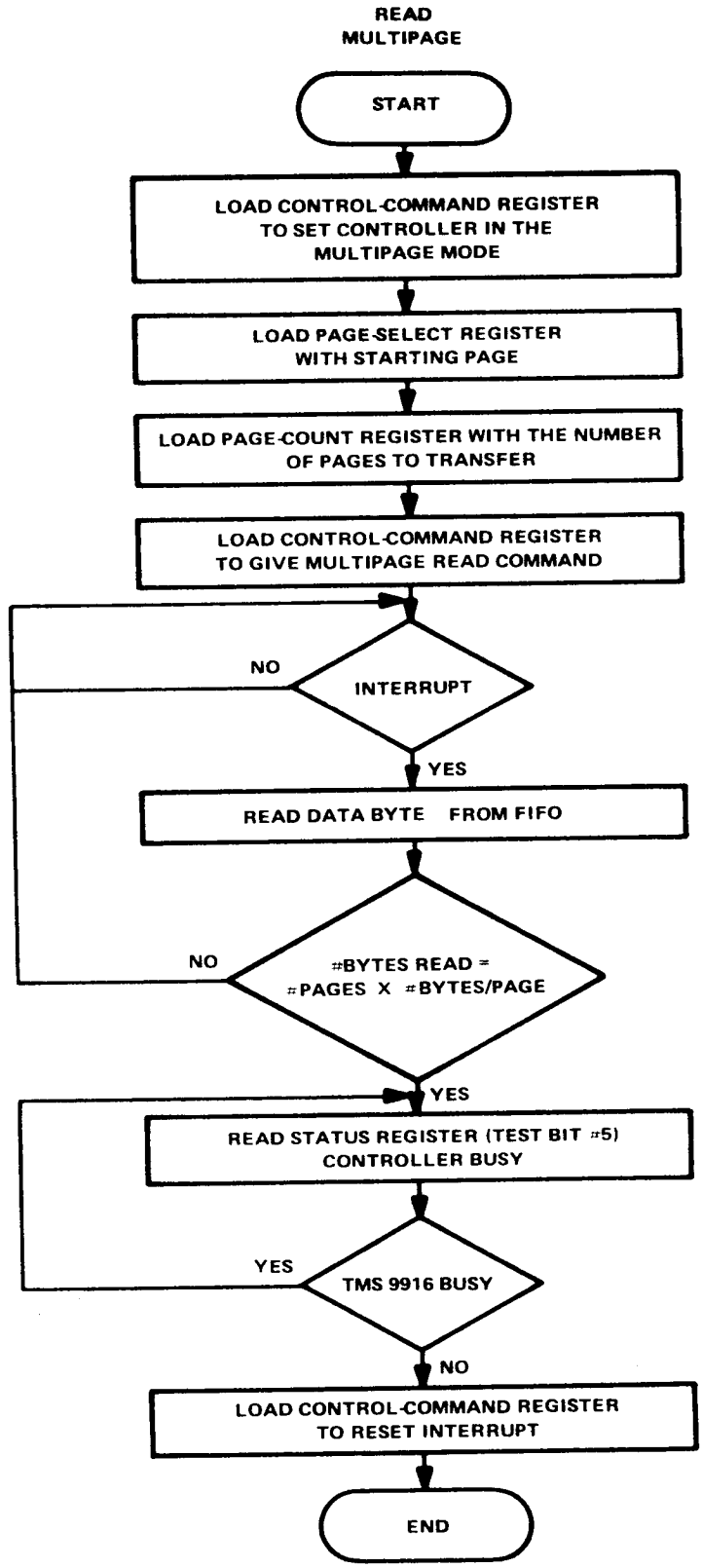
WRITE
SINGLE PAGE



WRITE
MULTIPAGE







4. TMS 9916 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage, V_{CC} (with respect to V_{BB})	−0.3 to 20 V
Supply voltage, V_{DD} (with respect to V_{BB})	−0.3 to 20 V
Supply voltage, V_{SS} (with respect to V_{BB})	−0.3 to 20 V
Input voltages (with respect to V_{BB})†	−0.3 to 20 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

†For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five (5) milliseconds without any damage to the device.

4.2 RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to 70°C

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, V_{BB}	−5.25	−5	−4.75	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	2.4		V_{CC}−1	V
High-level clock input voltage, $V_{\phi H}$	9		V_{DD}	V
Low-level input voltage, V_{IL} (all inputs except clocks)	−1		0.8	V
Low-level clock input voltage, $V_{\phi L}$	−1		0.6	V

4.3 STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to 70°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current (all inputs except clock and data I/O)	V_I = 5 V				10	μA
I_{IH}	High-level data I/O input current	V_I = 5.25 V,	CS = 0			150	μA
I_{IL}	Low-level data I/O input current	V_I = 0,	CS = 0			−150	μA
$I_{\phi IH}$	High-level clock input current	V_I = 12 V,	CS = 0			+50	μA
$I_{\phi IL}$	Low-level clock input current	V_I = 0 V,	CS = 0			−50	μA
I_{BB}	Supply current from V_{BB}	T_A = 25°C,	$t_{c(\phi)}$ = 500 ns			−1	mA
I_{CC}	Supply current from V_{CC}					100	mA
I_{DD}	Supply current from V_{DD}					50	mA
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = 400 μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 5.25 V,	I_{OL} = 1.9 mA			0.6	V
C_i	Capacitance, all input except clock					10	pF
$C_{i(\phi)}$	Capacitance, clock input					50	pF
C_o	Capacitance, output buffers					25	pF

4.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	0.48		2	μs
$t_{r(\phi)}$	Clock rise time (10% to 90%)	5		50	ns
$t_{f(\phi)}$	Clock fall time (90% to 10%)	5		50	ns
$t_{w(\phi1)}$	Pulse width, $\phi1$	75			ns
$t_{w(\phi2)}$	Pulse width, $\phi2$	200			ns
$t_{d(\phi1, \phi2)}$	Delay time, $\phi1$ to $\phi2$	0	5		ns
$t_{d(\phi2, \phi1)}$	Delay time, $\phi2$ to $\phi1$)	70			ns
$t_{dL(\phi1, \phi2)}$	Delay time, leading edges of $\phi1$ to $\phi2$	100			ns

NOTE: RESET can occur anywhere but must be held at least two clock cycles.
All switching lines are assumed to be at 10% or 90% values.

$T_A = 0°C$ TO $70°C$

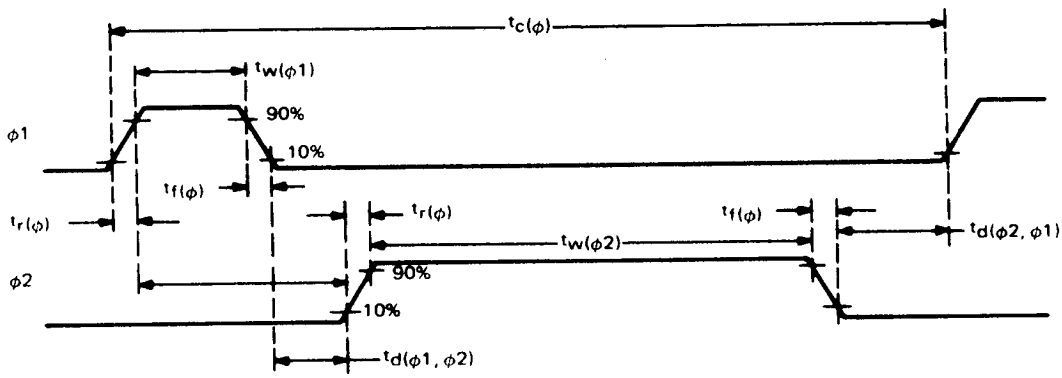
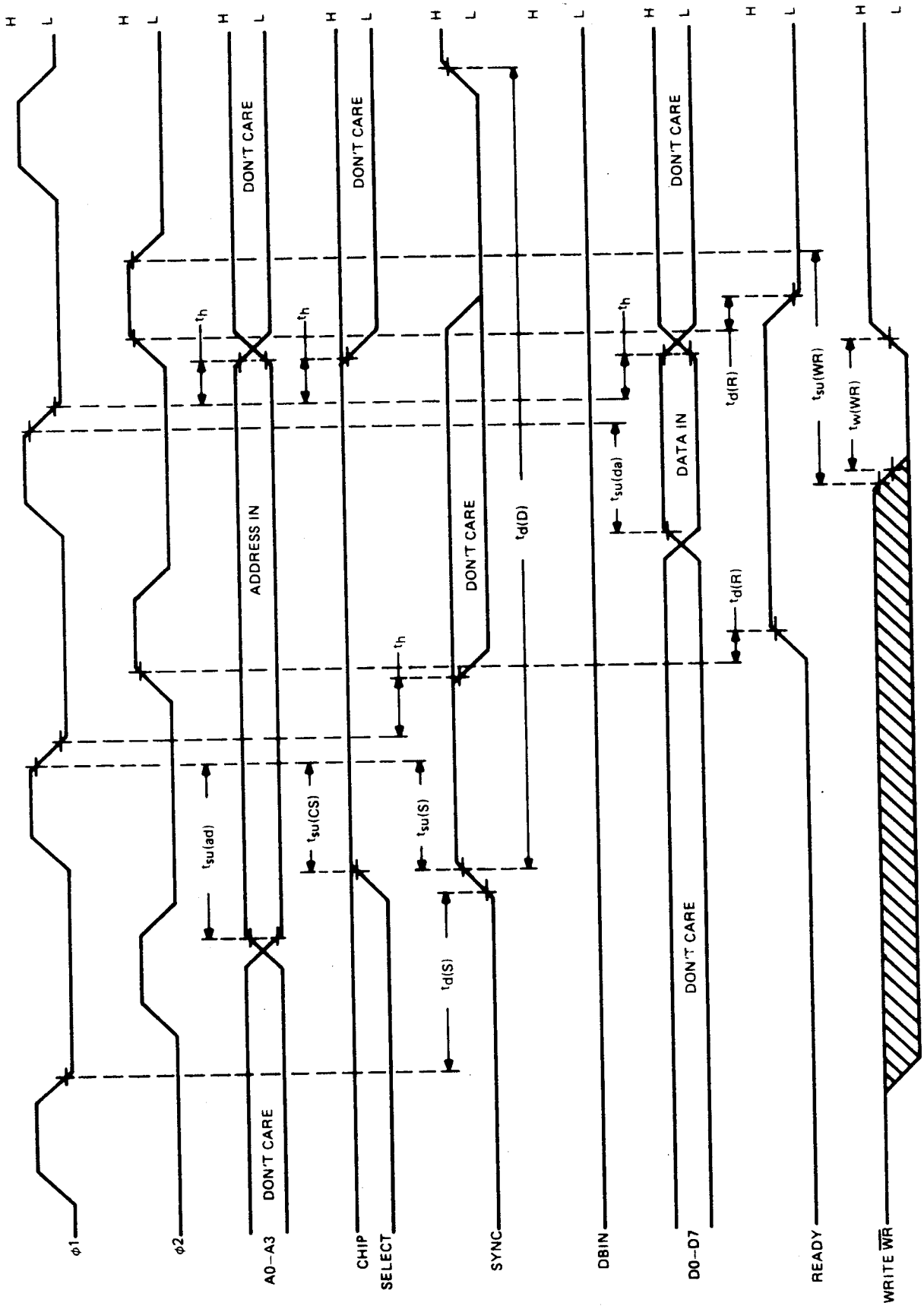


FIGURE 11 – CLOCK TIMING REQUIREMENTS

4.5 INTERFACE TIMING, $T_A = 0°C$ TO $70°C$

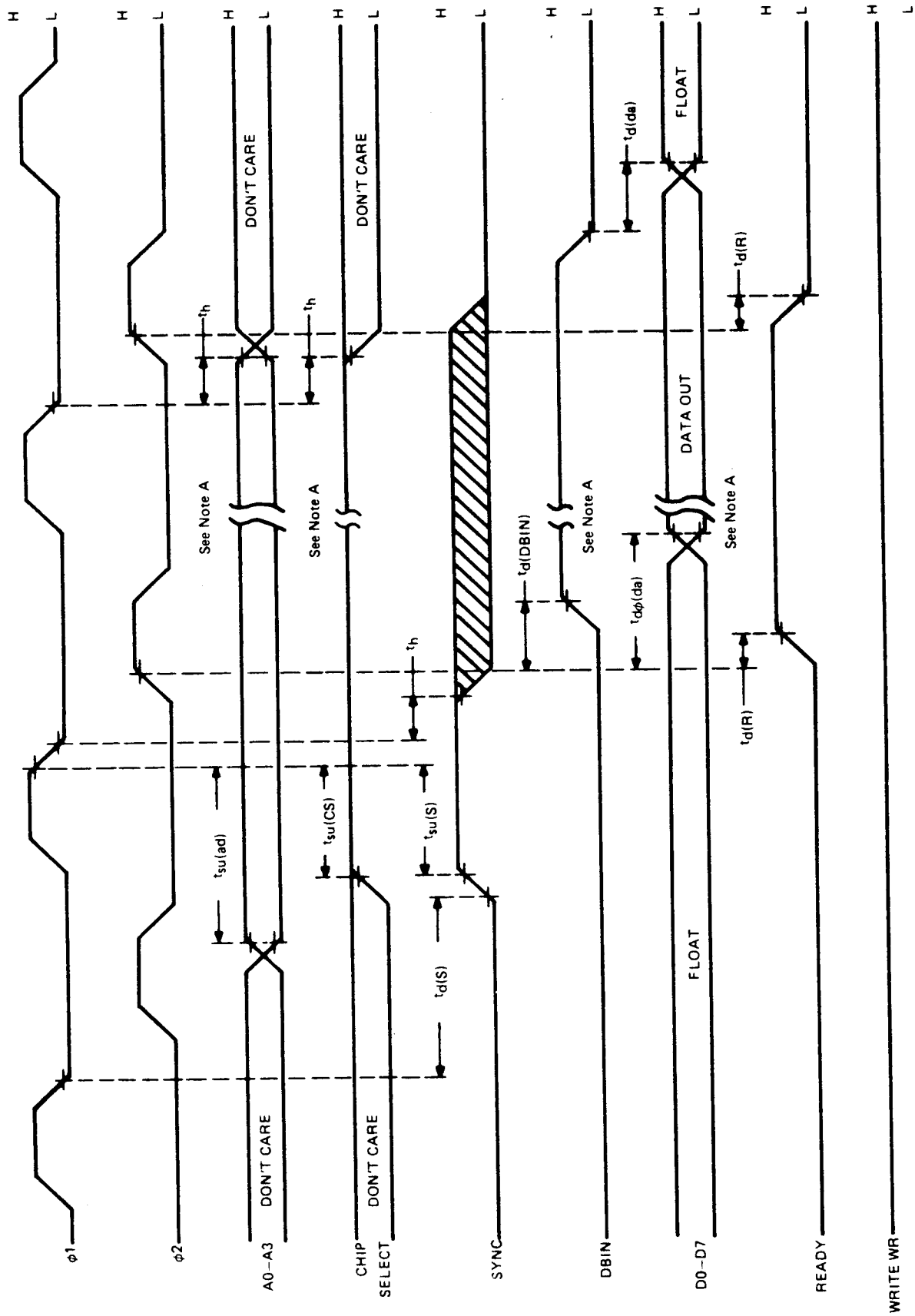
PARAMETER		MIN	NOM	MAX	UNIT
$t_{w(WR)}$	Pulse width, WR	$2/3t_{c(\phi)}$	480		ns
$t_{su(ad)}$	Setup time for address in $\phi1$ (falling edge)	125			ns
$t_{su(CS,S)}$	Setup time for chip-select and SYNC in $\phi1$ (falling edge)	105			ns
$t_{su(WR)}$	Setup time for WR input in $\phi2$ (falling edge)	160			ns
$t_{su\phi(da)}$	Data setup time in $\phi1$ (falling edge)	125			ns
t_h	Hold time from $\phi1$ (falling edge)	0			ns
$t_{d(\phi(da))}$	Data output delay time from $\phi2$ to valid (rising edge)			290	ns
$t_{d(da)}$	Data output delay time from DBIN to FLOAT			140	ns
$t_{d(DBIN)}$	DBIN input delay time into $\phi2$ (rising edge)			160	ns
$t_{d(R)}$	READY output delay time in $\phi2$ (rising edge)			100	ns
$t_{d(S)}$	SYNC input delay time from $\phi1$ (falling edge)	0			ns
$t_{d(D)}$	Delay time between SYNC "0" to "1" transitions	1.5			μs

NOTE: All timing specifications are in accordance with capacitive loading of 100 pF plus 1 TTL load on D0; D7 and 25 pF; 1 TTL load on all others.



Requires negative transition before $t_{su(WR)}$, then remains low for duration of $t_{w(WR)}$. WR must be active for valid data-in.

FIGURE 12 – WRITE CYCLE TIMING



NOTE A: Data out will remain valid as long as address and chip select remain valid.

FIGURE 13 – READ CYCLE TIMING

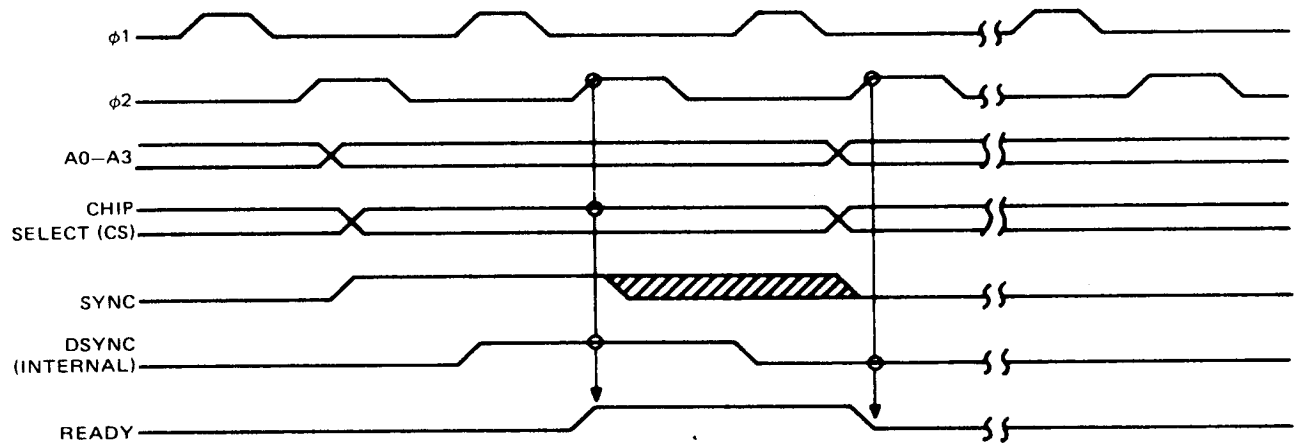


FIGURE 14 – RELATION BETWEEN READY, SYNC, AND CHIP SELECT

4.6 BUBBLE FUNCTION TIMING, T_A = 0°C TO 70°C

PARAMETER		MIN	NOM	MAX	UNIT
$t_{w(INIT)}$	INITRW pulse width	500			ns
$t_{su\Theta(da)}$	Setup time, data input from Θ1 (falling edge)	1000			ns
$t_{n\Theta(da)}$	Hold time data input from θ2 (falling edge)	1500			ns
$t_{d(GC50)}$	GC50 delay time from Θ1 (rising edge)	0		200	ns
$t_{d(INIT)}$	INITRW delay time from θ1 (falling edge)			200	ns
$t_{d(OUT)}$	Data output delay time from φ2 to valid data (rising edge)			500	ns
$t_{d(FUN)}$	Funcen delay time from GC50 (falling edge)			500	ns
$t_{d(\Theta1, \Theta2)}$	Delay time from φ2 (rising edge)			200	ns

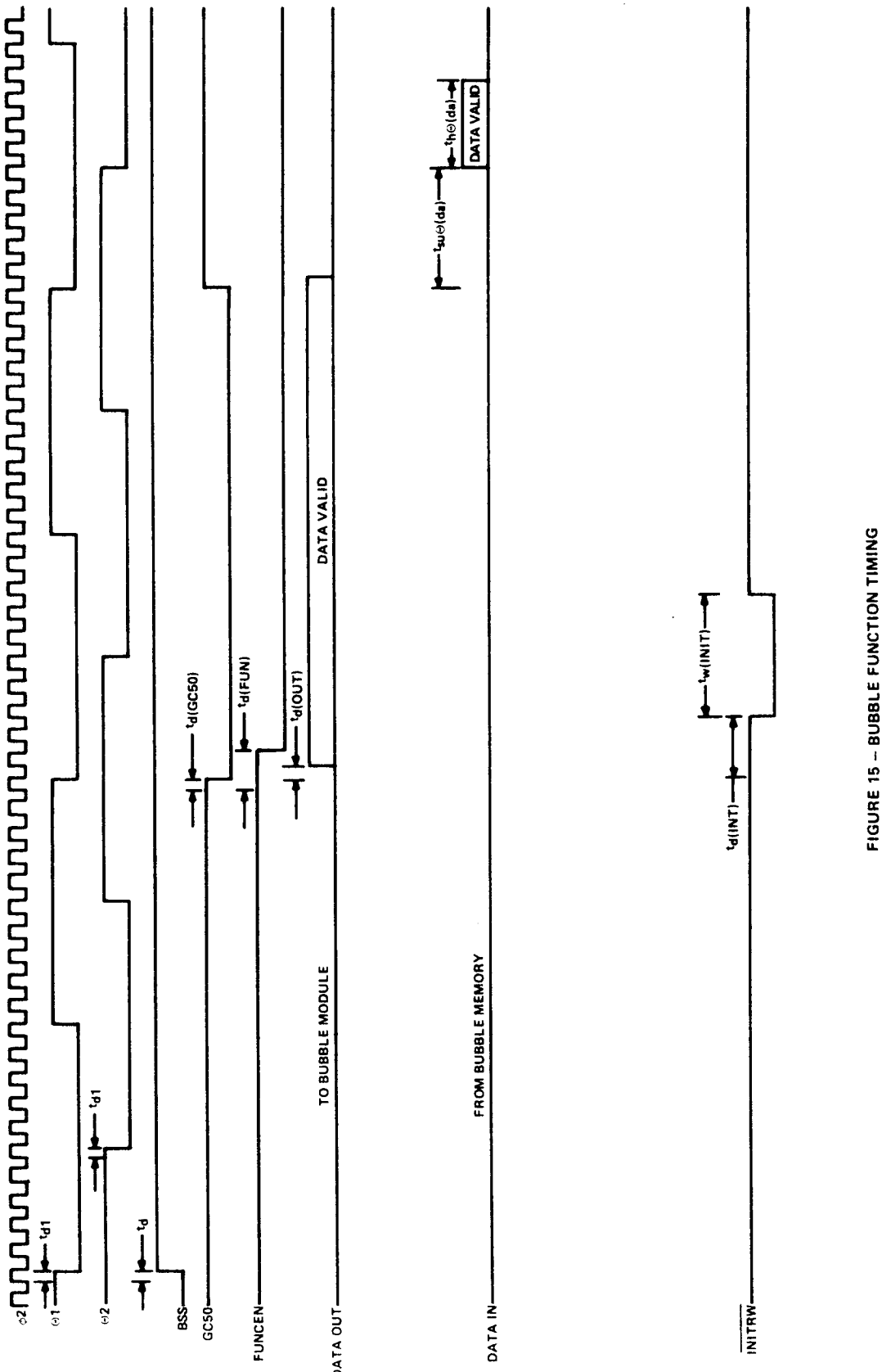
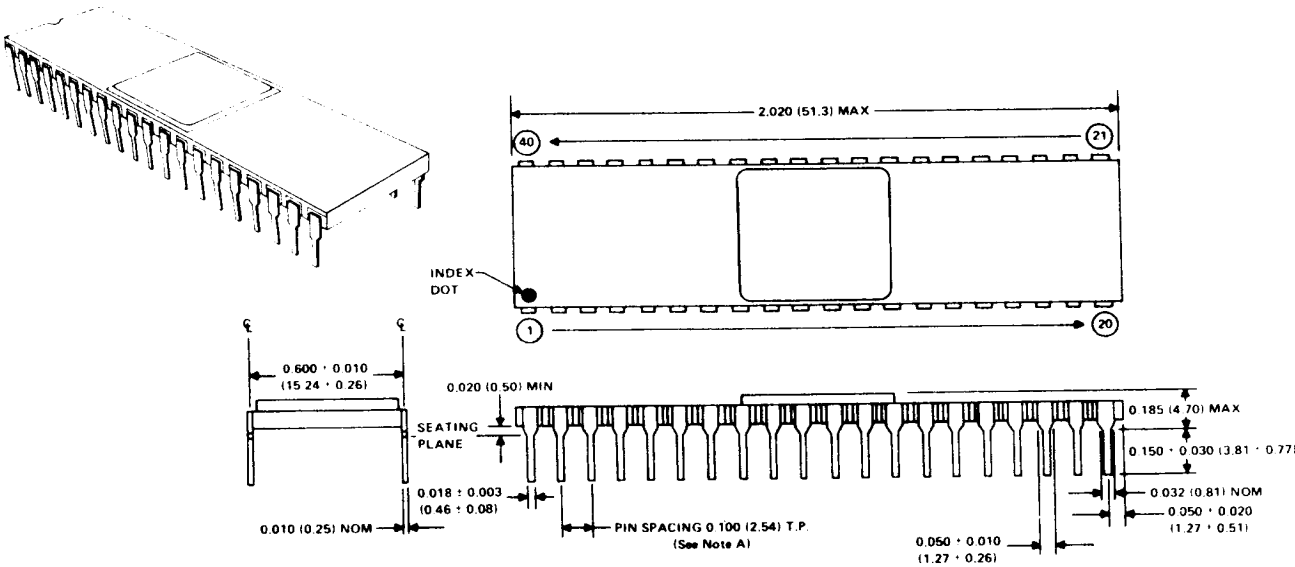


FIGURE 15 – BUBBLE FUNCTION TIMING

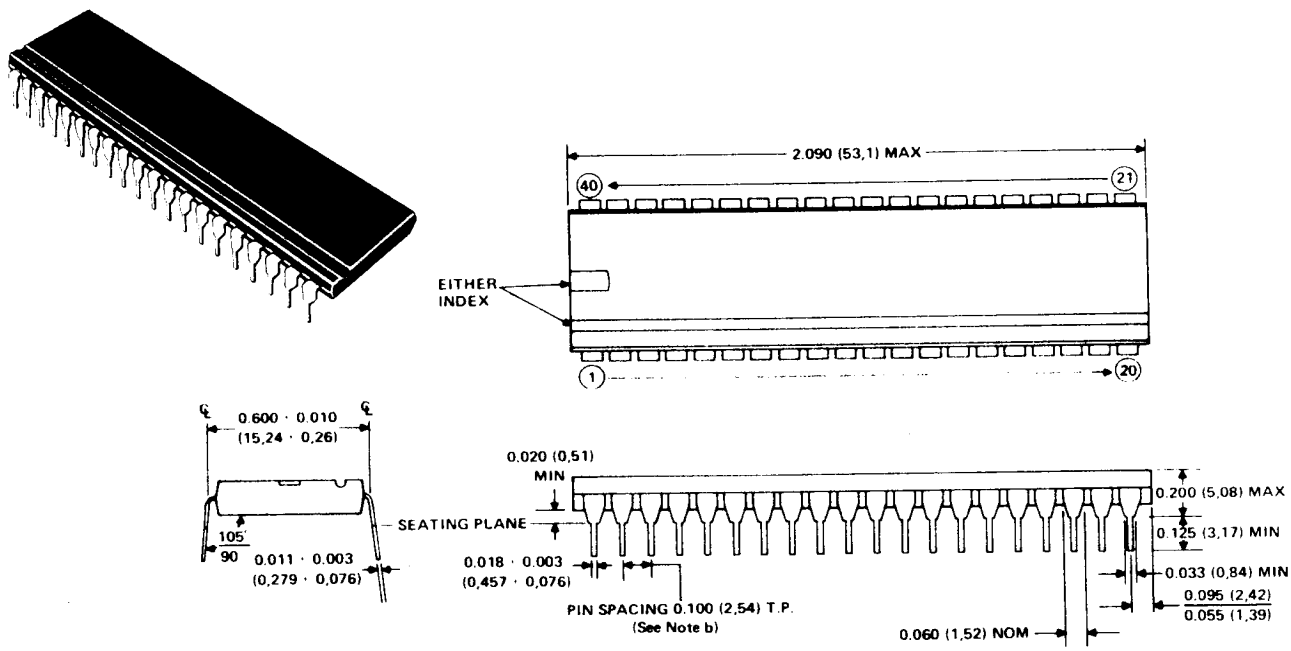
5. MECHANICAL DATA

5.1 TMS 9916 – 40-PIN CERAMIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

5.2 TMS 9916 – 40-PIN PLASTIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.25 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.